FE-I1 Measurements

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Chopper Performance

- Further studies of charge and timing performance of charge injection

Ganged Pixel Crosstalk

- Crosstalk couplings for all pixels in ganged region

Double Pulse Resolution

- Study efficiency for readout of double pulses using single chip assembly

Double Trigger Studies

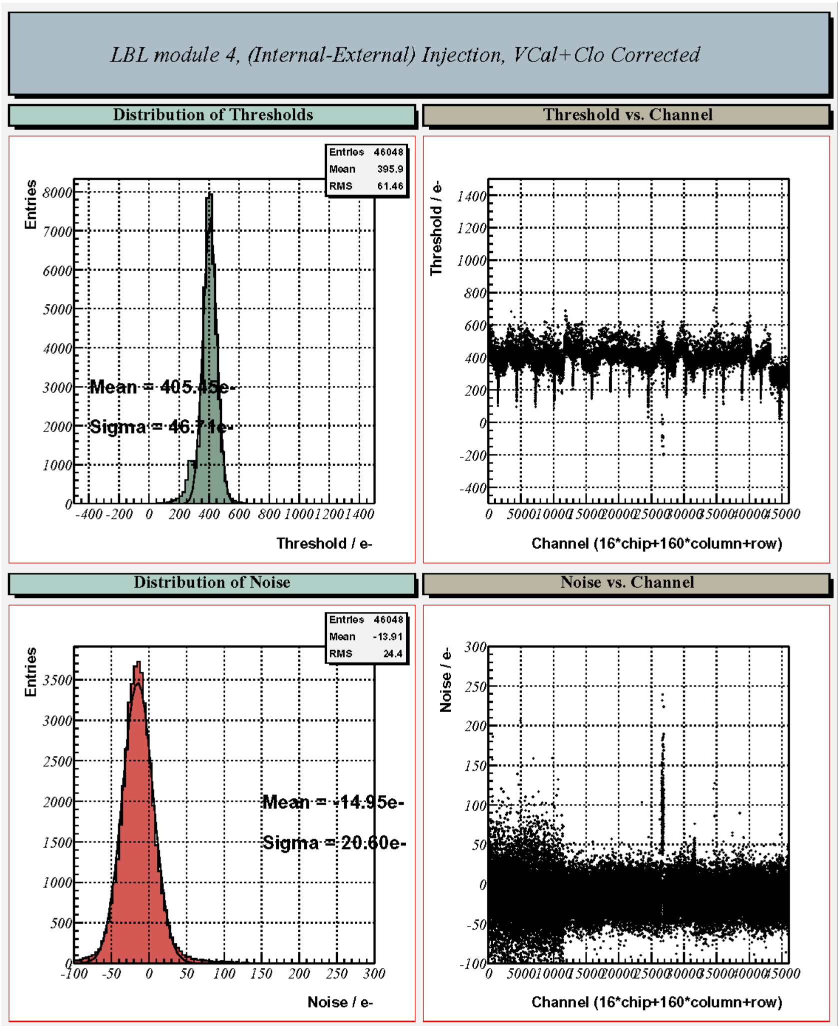
- Look for digital crosstalk using two independent groups of triggers

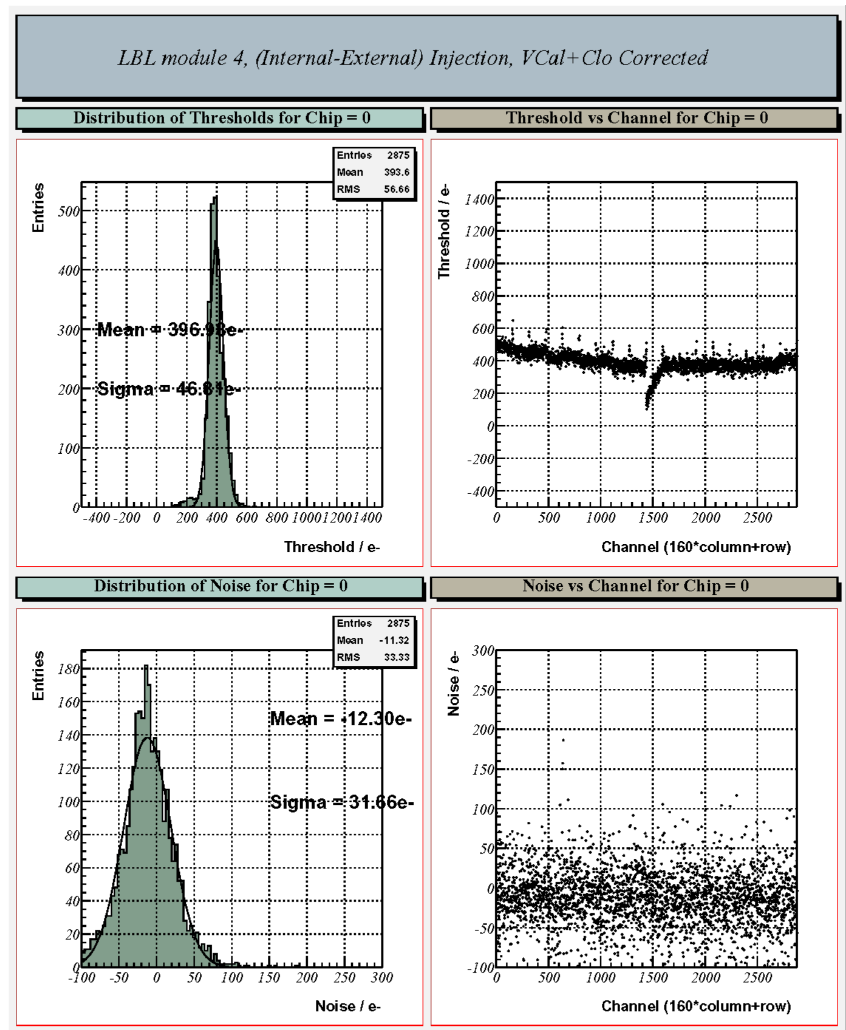
In-time Threshold Studies

- Use Event Filter in TPLL to study single crossing threshold as a function of timing

Chopper Performance

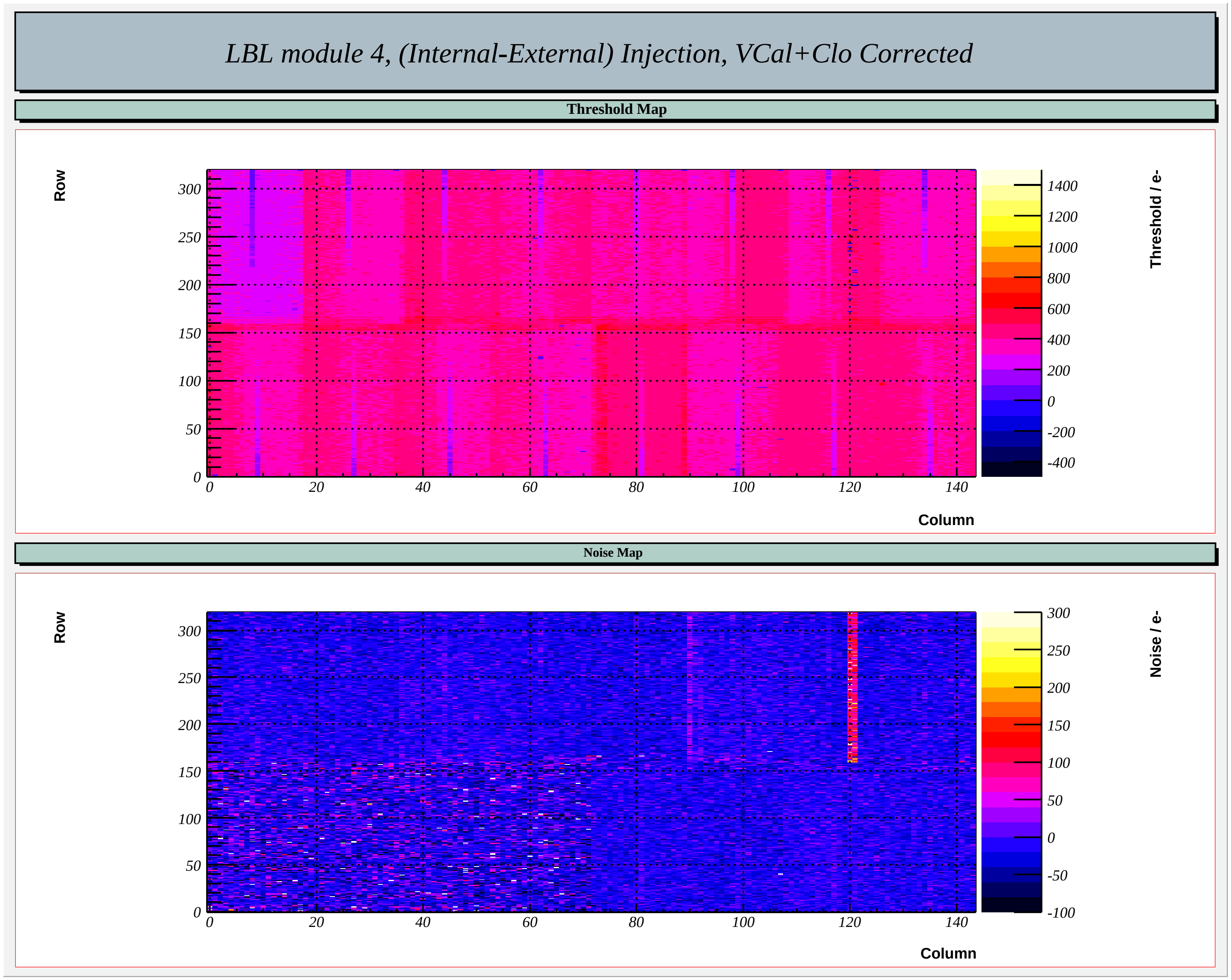
- Compare performance of internal and external injection systems for charge (TOT) and timing (timewalk) measurements.
- Reminder of performance observed in module threshold scans:





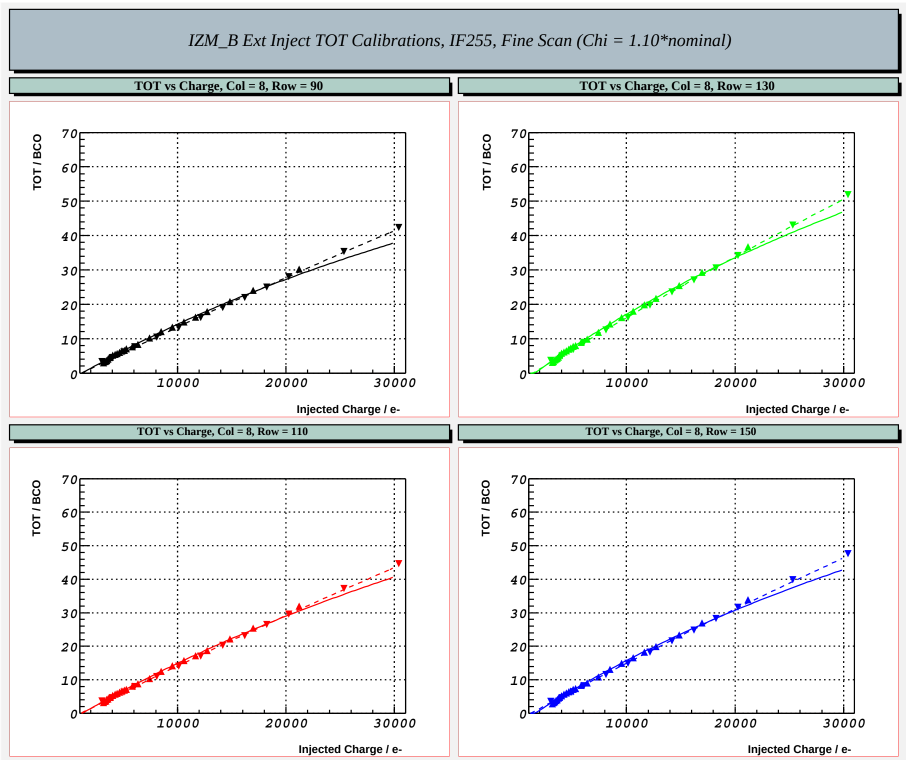
- Systematic offset between internal and external injection plus "Column 9 effect".

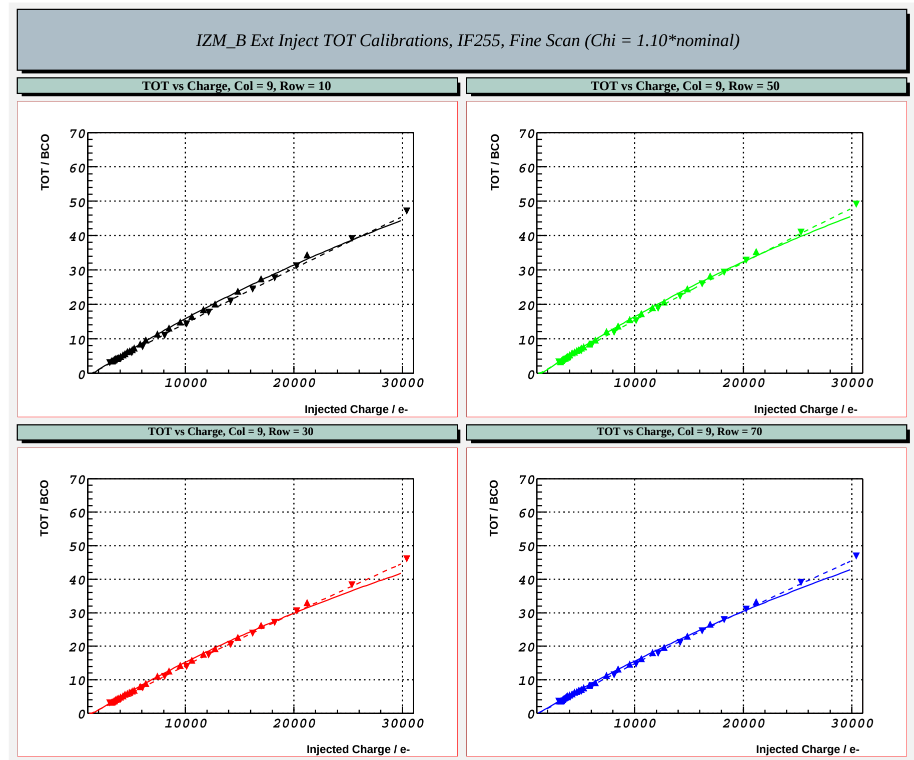
• Overall map of module shows uniformity of offset in each chip, excepting Column 9:



• Study this issue in more detail using TOT information to estimate injected charge.

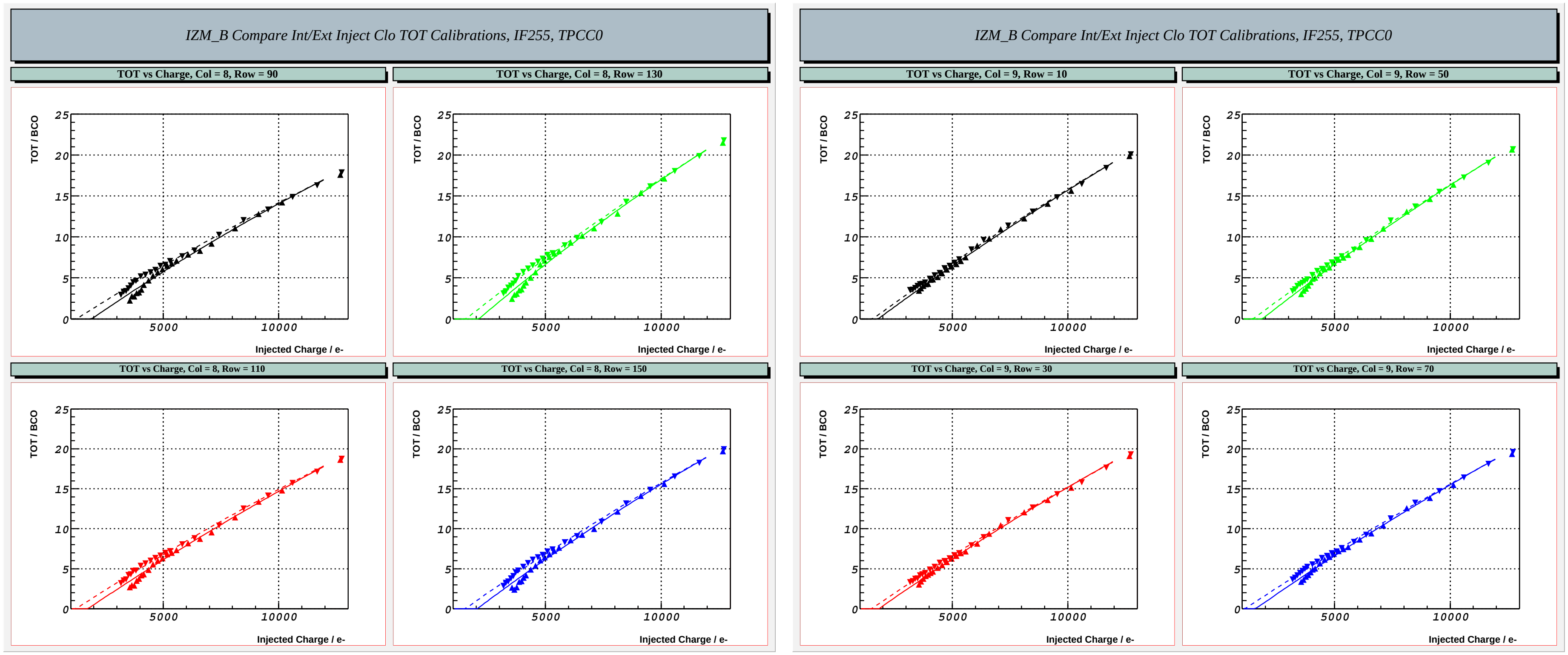
- First compare Clo and Chi scales for external injection:





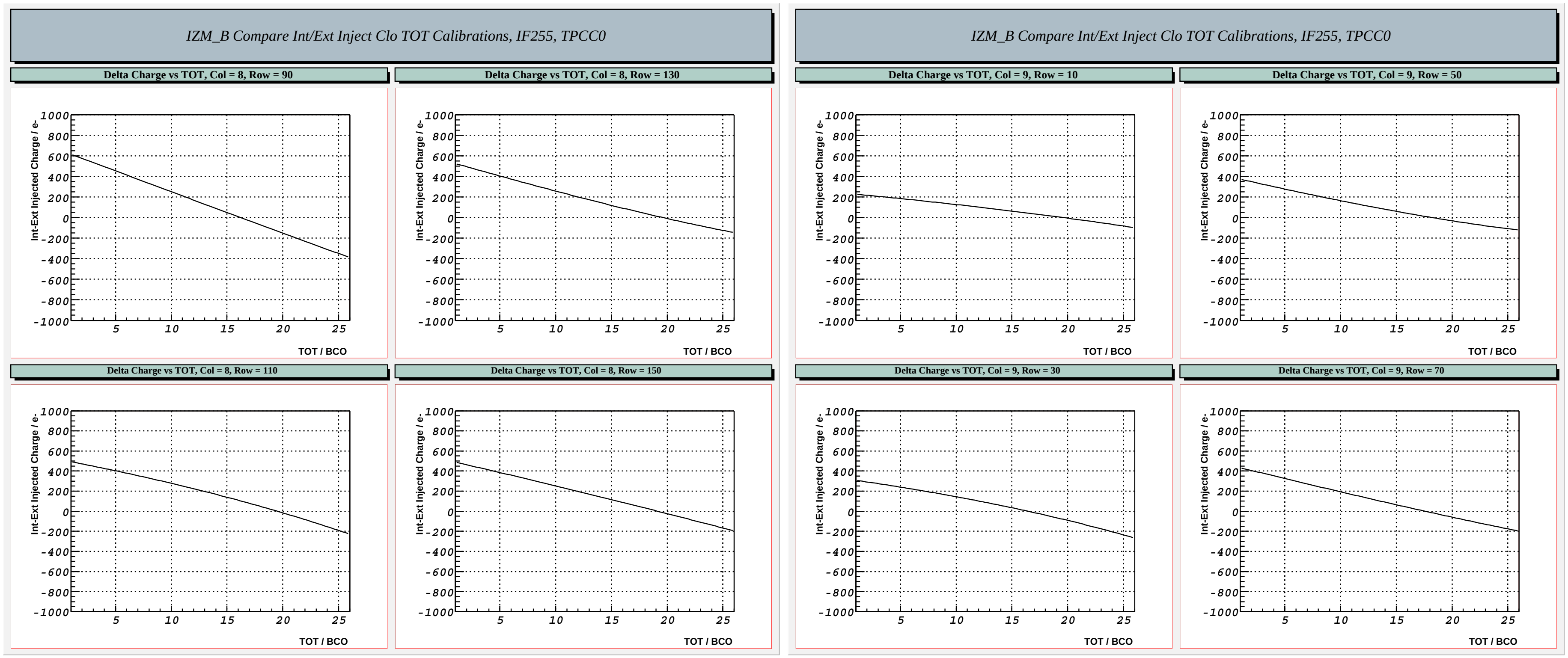
- Agreement between two ranges is fairly good if Chi is rescaled by a factor 1.10 (shown here).
- Some ideas about why CapMeasure might underestimate Chi, but not conclusive.
- Present bump pad layout could be improved to eliminate coupling from Cfb to Chi using full six metals, but we chose to keep FE-I1 pad design to insure capacitances did not change.
- Believe the present CapMeasure scheme is the best we can do without major changes, so FE-I2 will be the same.

- Next compare Clo scale for internal and external injection (critical scale):



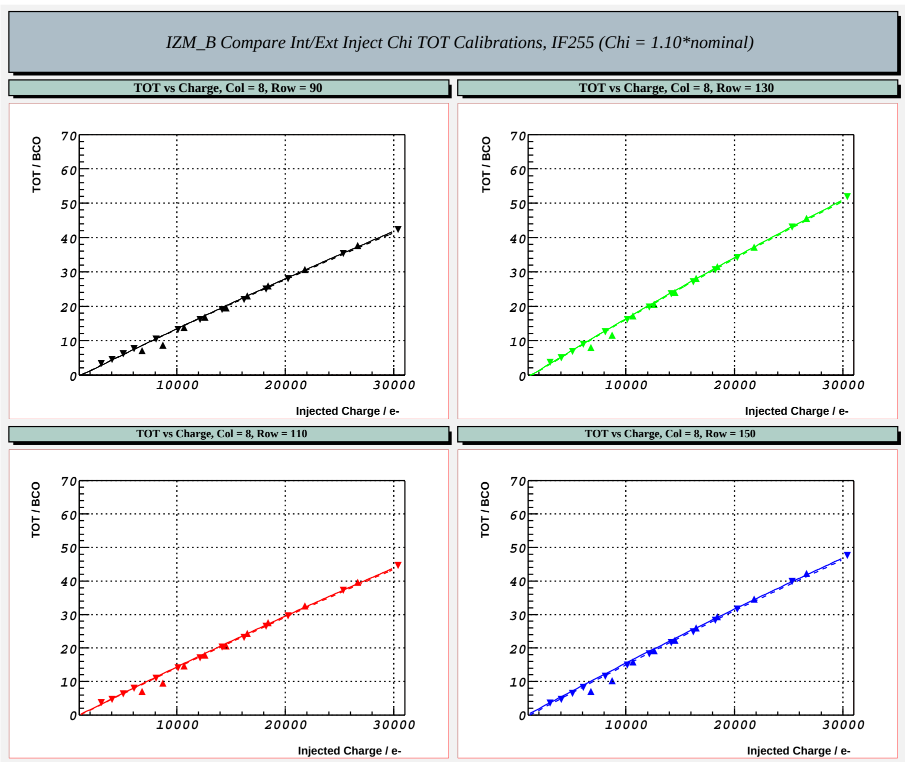
- Observe interesting effect, correlated strongly with behavior of internal and external threshold scans.
- First, observe non-linear difference (not an offset), which is about 400e at 3-4Ke where threshold measurements are made. It is almost zero above about 7Ke.
- Note that upper left plot in right group is the very bottom of Column 9, where the internal-external threshold difference is the smallest. Once the top of column 9 is reached, all of the rest of the array is relatively uniform (shows the same behavior).
- There is also a small non-linearity in the TOT itself as it approaches threshold.

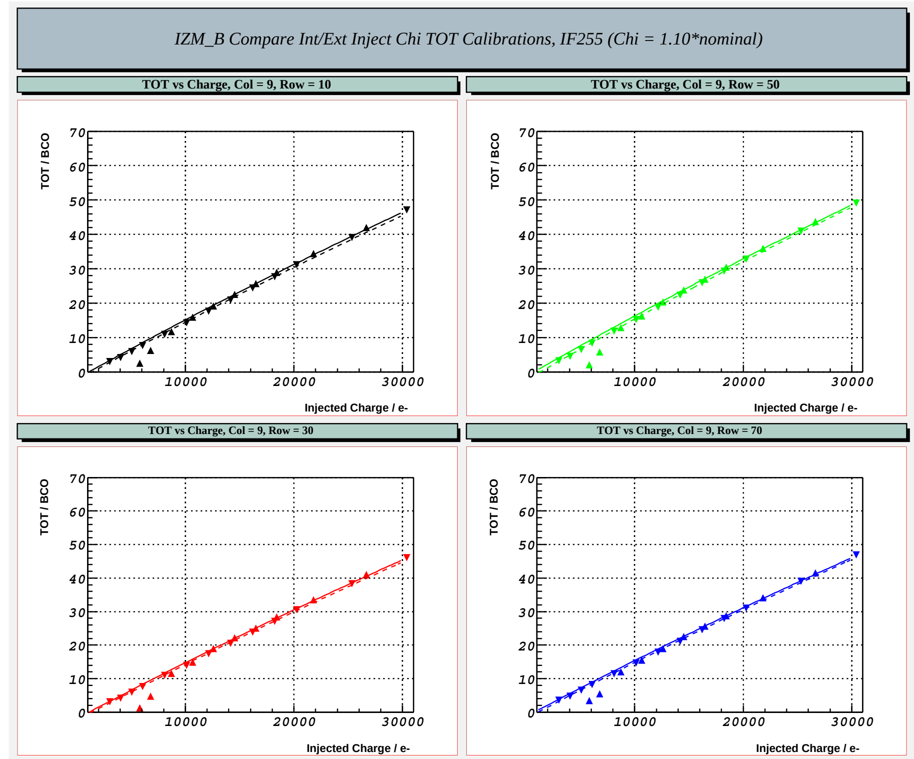
- Compare difference between fit curves in non-linear region:



- Observe that fits agree well at bottom of Column 9, and show larger differences everywhere else. For reference, 5Ke is about TOT=7, and 10Ke is about TOT=15.
- Internal injection distribution: VCal DAC and I->V mirror are located at the bottom of Column 9. VCal voltage is brought to top of this column, and then bussed across the top, finally descending into individual columns. This is the only special feature of Column 9, but we have no detailed model of why VCal varies along Column 9.
- FE-I2 has VCal trace resistance reduced by factor 4 and completely shielded Str/ Strb distribution within pixel. Both changes may be significant for the chopper.

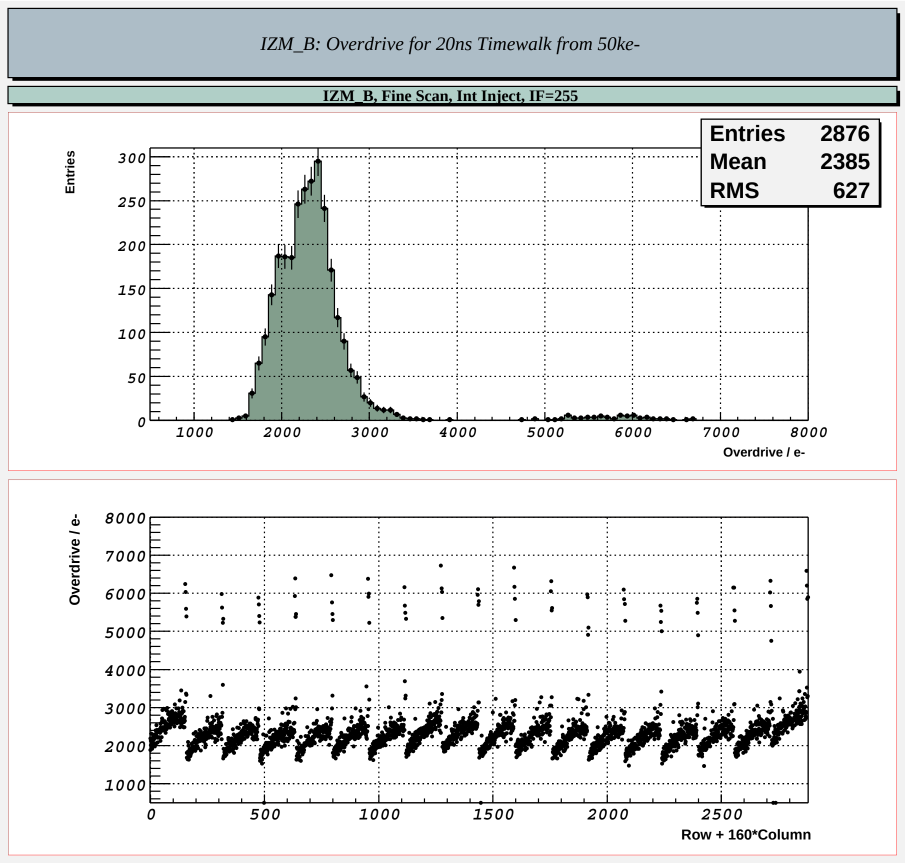
- Compare Chi scale for internal and external injection:

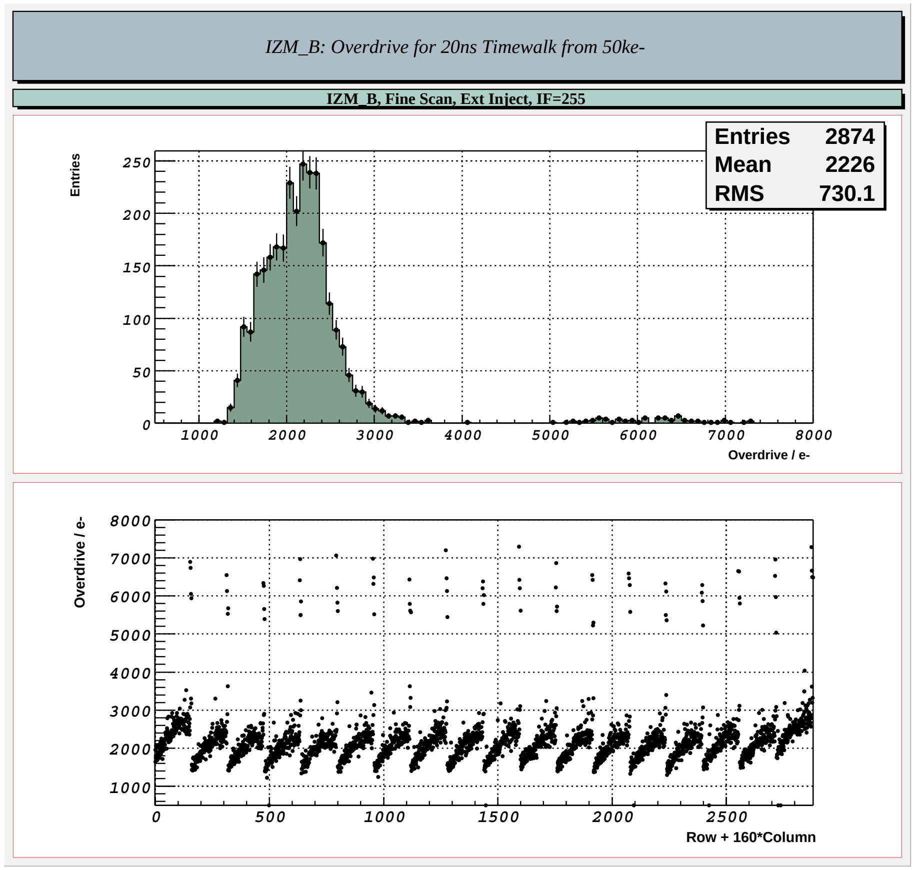




- Agreement in region where VStep is equal (5Ke on Clo scale is about 45Ke on Chi scale) is good - no sign of non-linearity. However, internal injection efficiency falls to zero below about 8Ke, whereas external injection is linear to the origin. This is not understood.
- Layout for FE-I1 does show significant coupling from Str to Clo VStep, and perhaps this is the explanation (no simulations performed) for the Clo non-linearity (should give offset ?).

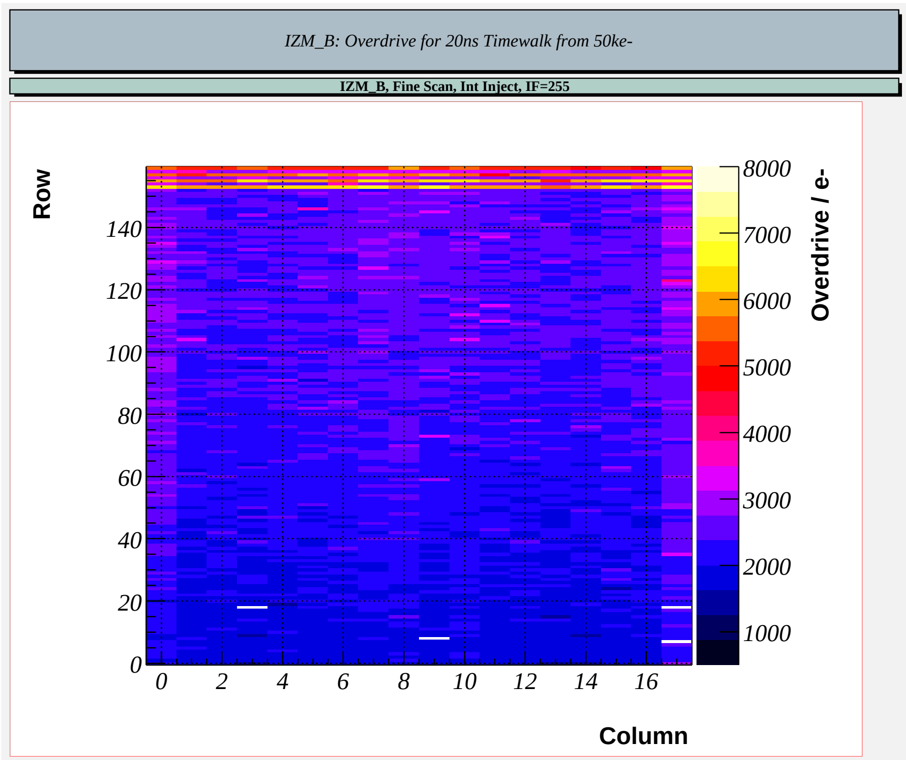
- Study performance of injection for timewalk scans (left = Int, right = Ext):

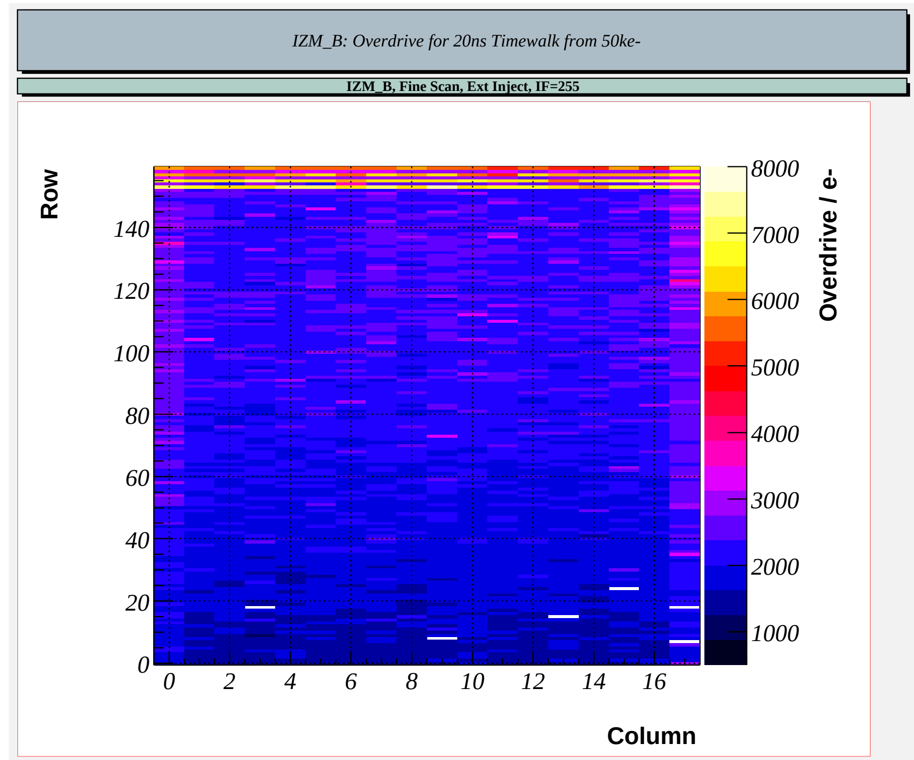




- Minor differences observed between internal and external scans, but overall results are very comparable.
- For internal injection, ganged pixels have a lower timewalk, but normal pixels have slightly worse timewalk.

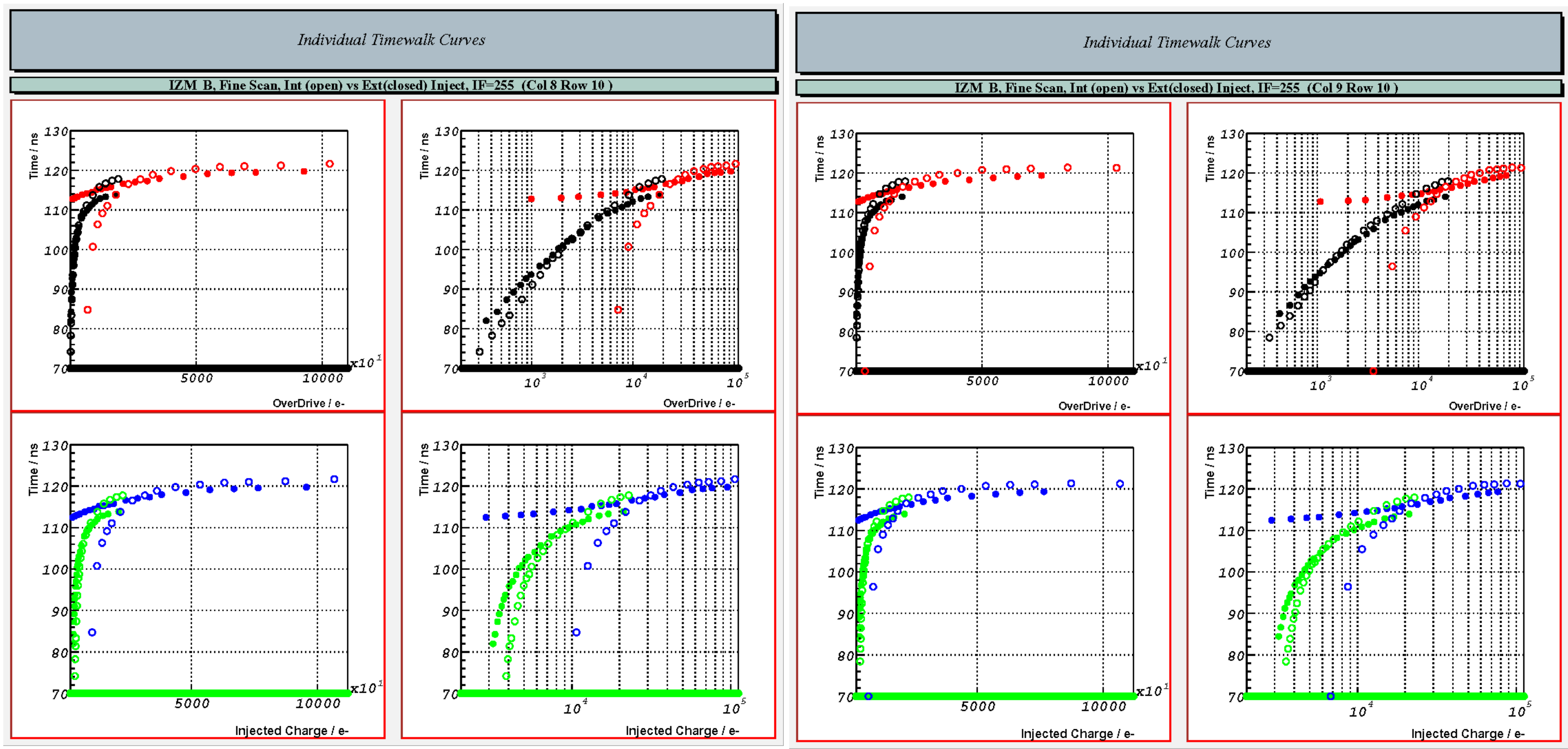
- Compare timewalk maps (left = Int, right = Ext):





- External injection shows lower timewalk for small row numbers and higher timewalk for ganged pixels.

- Compare individual timewalk curves (vertical axis is Str Delay in nsec):



- Upper right of four plots is easiest to interpret. It shows reasonably good agreement over the full Clo scale. There is also reasonable agreement for large VStep on the Chi scale. This means that the timewalk (overdrive) measurement should be comparable, because it only involves large VStep in Chi and small VStep in Clo.
- Major surprise is large deviation for small VStep on Chi scale. In internal injection, this is roughly the charge where the TOT also looses efficiency. The “fast” performance for external injection is bizarre, but may be due to Cfb - Chi coupling.

Summary of Chopper Measurements:

Charge Injection Performance:

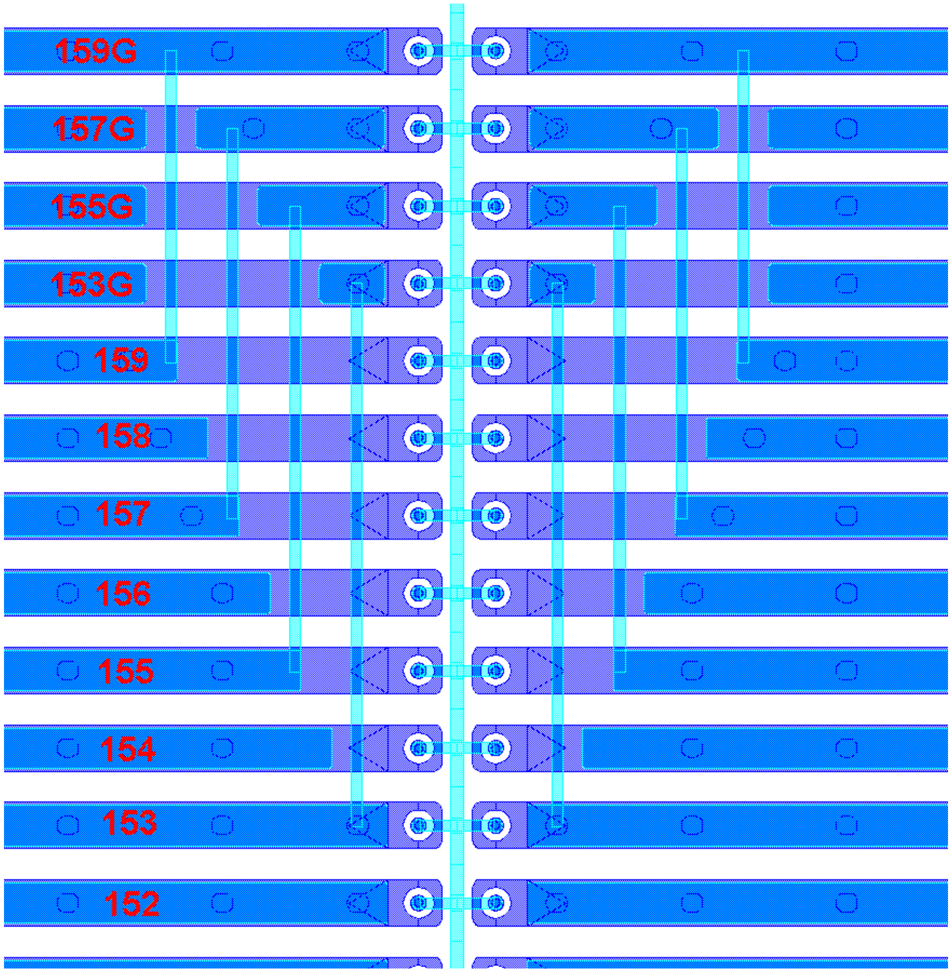
- Offset of roughly 400e observed between internal and external injection. No detailed understanding of this problem, but it may be related to crosstalk within the pixel between Clo and Str. Shielding of Str and Strb is much improved in FE-I2.
- Linear variation of offset observed in Column 9, which is the column containing the VCal DAC, and has the trace which brings VCal to the top of the chip for distribution. Again, no detailed model of the problem, but trace resistance has been reduced in FE-I2, and decoupling on VCal will be improved.
- These effects are large enough to be a nuisance, and could get worse with increased Clo used in FE-I2 (8fF instead of 4.6fF).
- The Chi scale develops poor efficiency in internal injection for small VStep.

Timing Performance:

- Agreement between internal and external injection timewalk measurements is reasonably good. Module timewalk measurements agree with single chips.
- Agreement in timing performance on Clo scale is good for all VStep values.
- Timing performance for small VStep on Chi scale is very peculiar. In particular, the external injection case does not make sense. This could be a “feed-forward” problem related to the coupling of Chi and Cfb in the pad stack. This has not been studied in detail, and is not improved for FE-I2.

Ganged Pixel Crosstalk

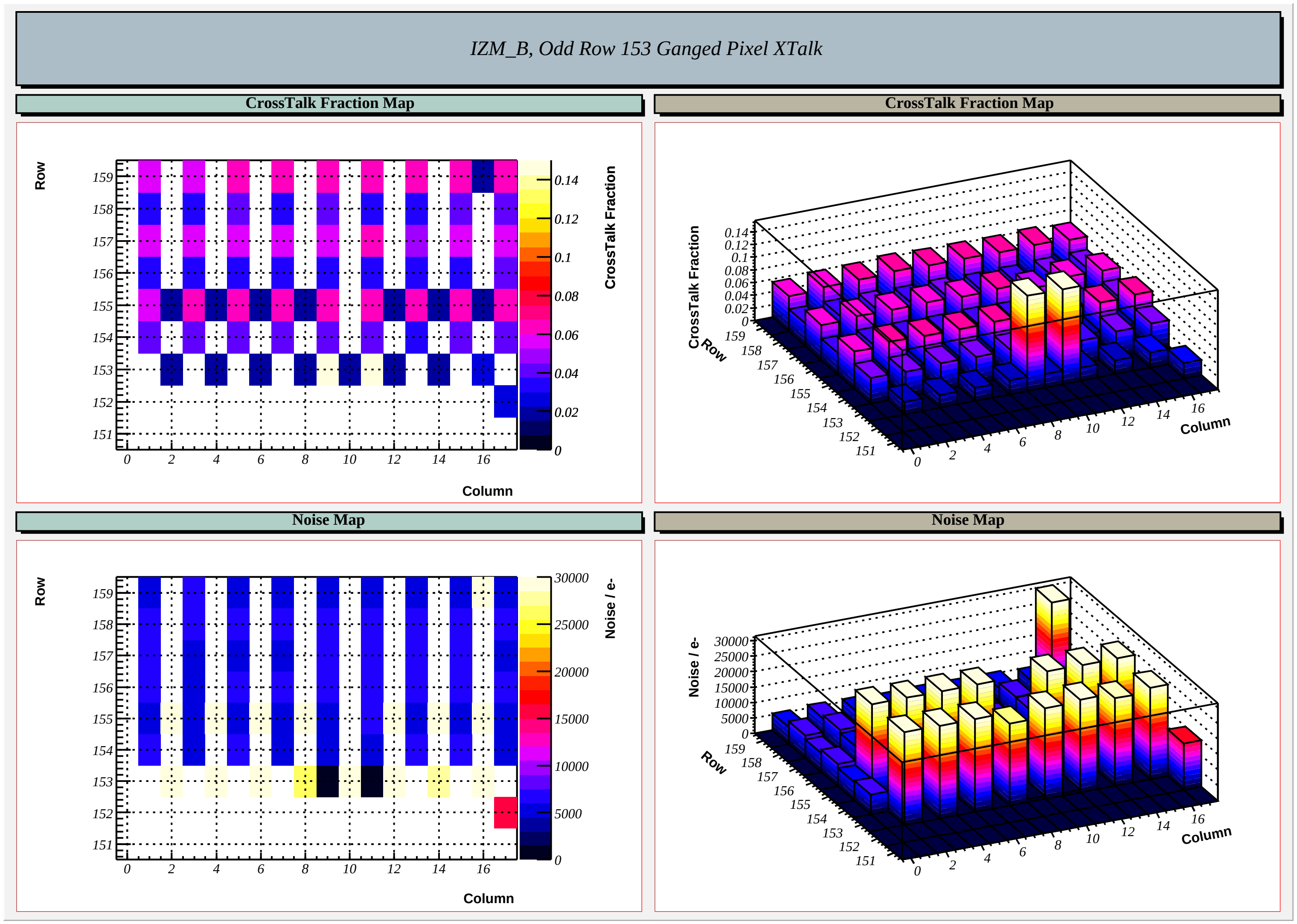
- Observe very different performance for ganged pixels, depending on whether they are connected with AMS bumps or IZM bumps (see module meeting).
- Basic measurement is to look at the cross-talk fractions to all neighboring pixels in the ganged region. Use an IZM single chip to do this (IZM_B).
- Reminder of geometry:



Sources of cross-talk for pixel 153:

- Inter-pixel capacitance to pixels 152 and 154, and 159 and 155G
- Capacitance between metal trace and pixel implant for pixels 154, 155, 156, 157, 158, 159, and also for 155/155G, 157/157G, 159/159G.
- Capacitance between metal traces for 155/155G

- Do Xtalk scan with VDDA=1.8V and use external injection with scan range up to DeltaVCal = 26000 (almost 1V VStep range).
- Example scan, injecting Row 153 in Odd Columns (nine pixels):



- Inject nine pixels (do not read them out) and 71 other pixels respond !

- Results for Odd Column scans for normal ganged pixels (not column 0 or 17). Also ignore nearest neighbor crosstalk between columns (it is typically less than 1%):

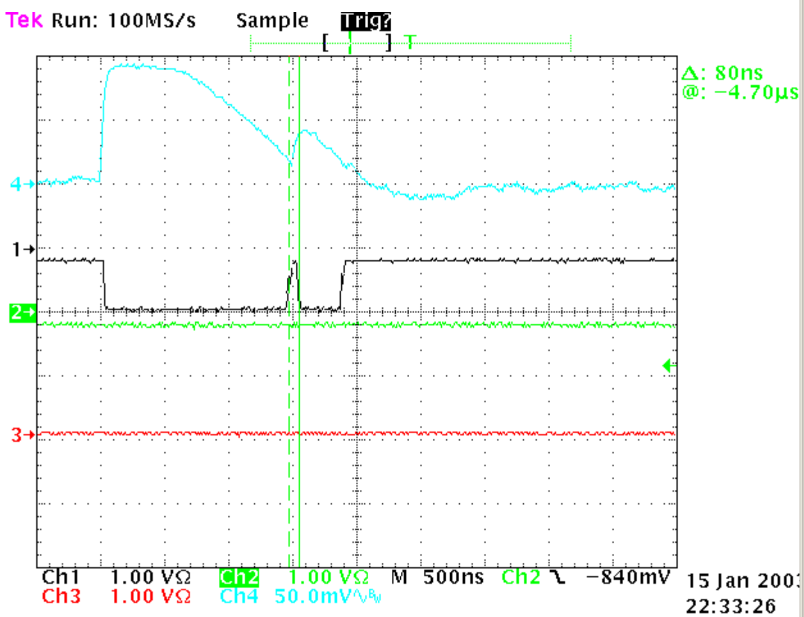
	152	**153**	**154**	**155**	**156**	**157**	**158**	**159**
151	1.7%							
152	-----							
153	1.7%	-----	6.1%	6.2%	5.3%	6.3%	5.2%	6.6%
154		4.2%	-----	1.6%				
155		6.3%	1.7%	-----	6.0%	6.8%	5.2%	6.6%
156		3.7%		4.3%	-----	1.9%		
157		5.8%		6.4%	2.0%	-----	5.6%	7.2%
158		3.8%		3.8%		4.5%	-----	2.0%
159		6.2%		6.2%		7.0%	2.5%	-----

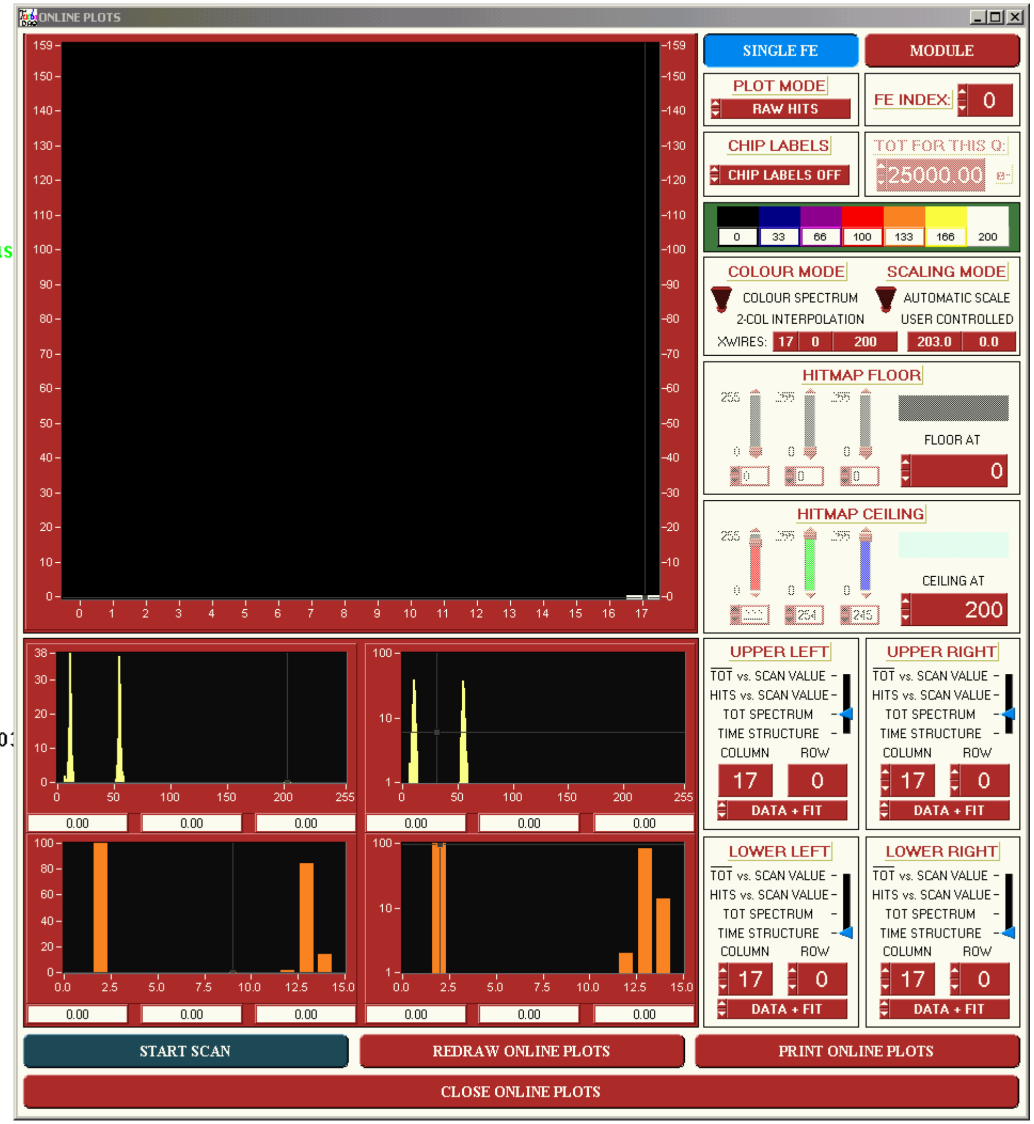
- Crude summary: interpixel crosstalk is about 2%, coupling between ganged and inter-ganged pixels is about 4%, and coupling between ganged pixels is about 6%.
- Summed crosstalk for ganged pixels (including nearest neighbors) is about 35%. Note in worst case, for a 3Ke threshold, need about 50Ke to fire additional pixels, so only the Landau tail should produce multiple hits in the ganged region.

Double Pulse Readout Studies

- Previously showed behavior of test pixel when injected with double steps using external injection. These measurements showed that the front-end is very linear and has excellent double pulse resolution, given by the time it takes the first pulse to return to threshold (not baseline).
- Use the double step injection system to study the combined front-end and readout performance of a singe chip (IZM_B). Compare performance with CEU=40MHz to slower column clock speeds.
- First, study case of a normal pulse followed by a small pulse. Use two groups of 8 trigger accepts and set the gap between the groups to be appropriate for the double pulse separation. Read out only one pixel to simplify the effects of the readout behavior.
- Second, study case of two large pulses with a larger separation, and adjust the separation to allow for readout of the full array. For a 32_step mask, and CEU=40, reading 10 hits per column pair requires 500ns, so this is an appropriate gap.
- **Note on pixel hit logic:** if a second hit arrives while the hit logic is waiting for a first hit to be transferred to the bottom of column, it is ignored. However, the hit logic is not edge-sensitive, so once the hit logic busy condition clears, it will begin processing the second hit if the discriminator output remains high. This will result in the hit being detected with the wrong leading edge timing. Although this behavior is not ideal, it occurs at a low rate, and would have been complex to eliminate.

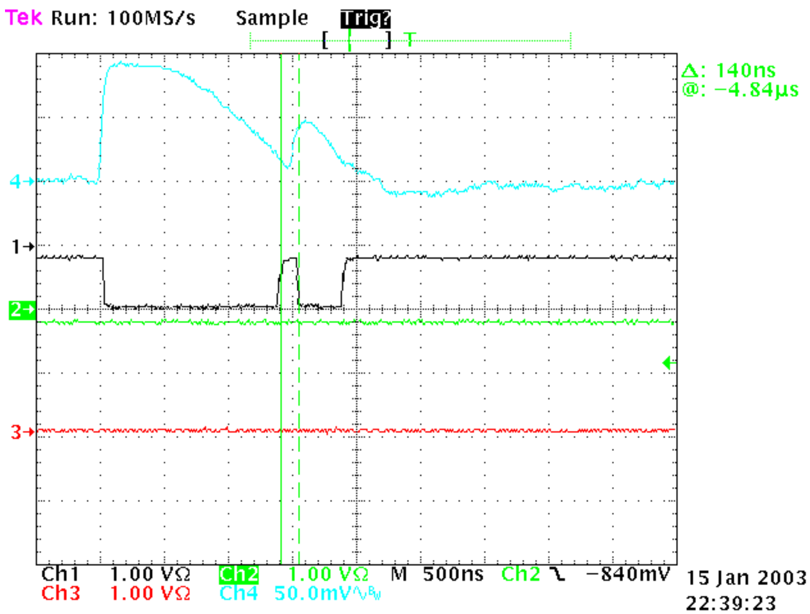
- Example of injection into testpixel only (single pixel to read out, 20Ke and 6Ke):

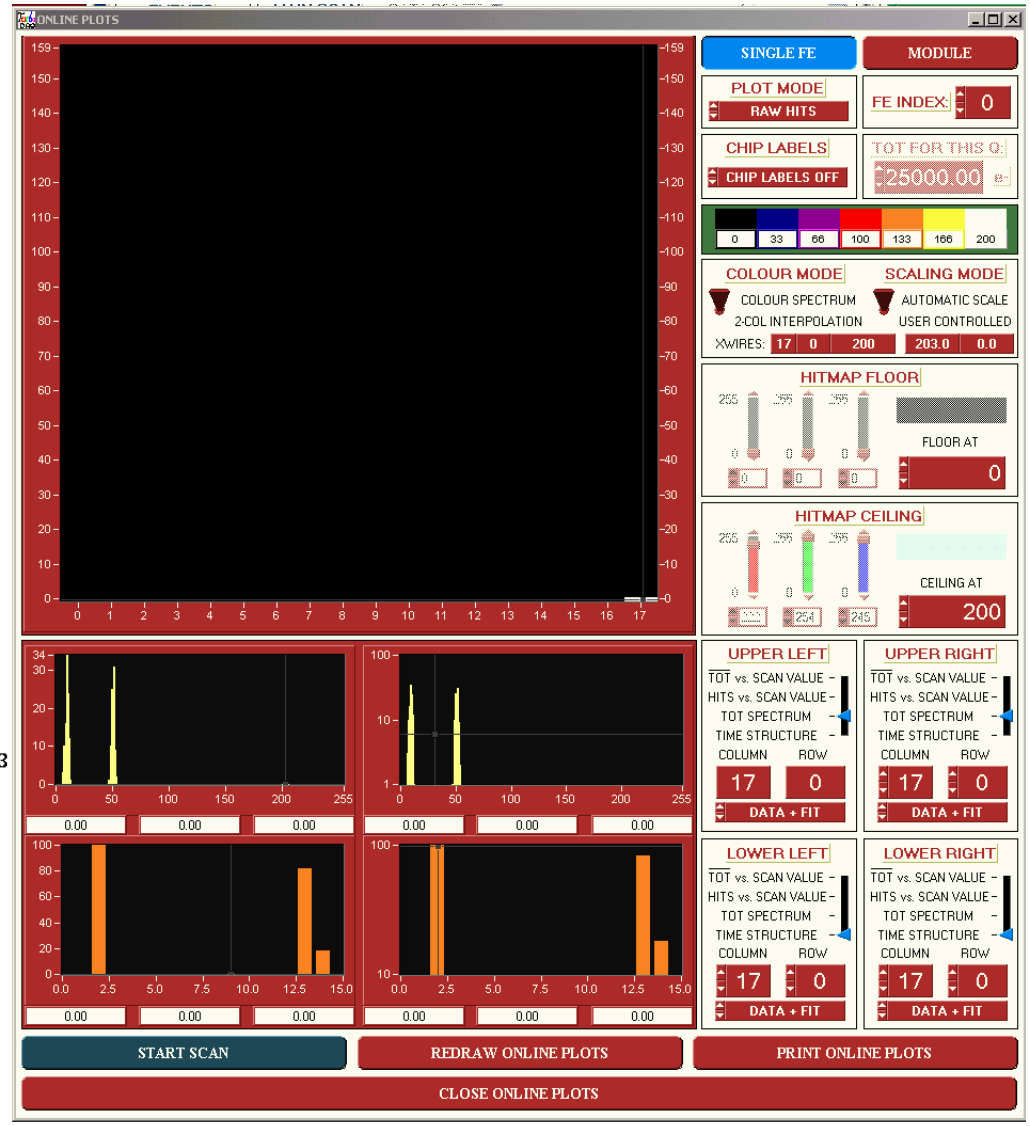




- In this case, the gap between pulses is only 80ns, but for a single pixel to read out, the double hits are both detected with 100% efficiency. The timing information on the second hit is slightly smeared/delayed due to the pixel being busy sometimes.

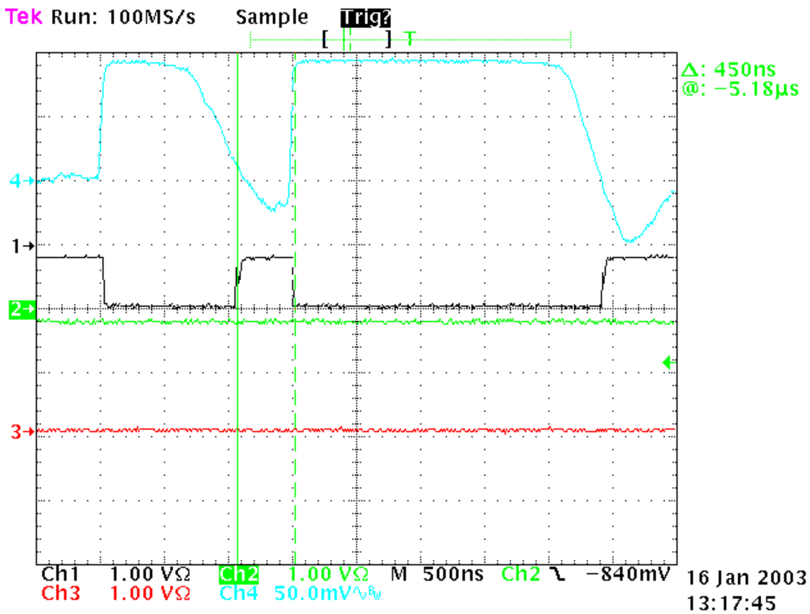
- Example of injection into testpixel only (single pixel to read out, 19Ke and 6Ke):

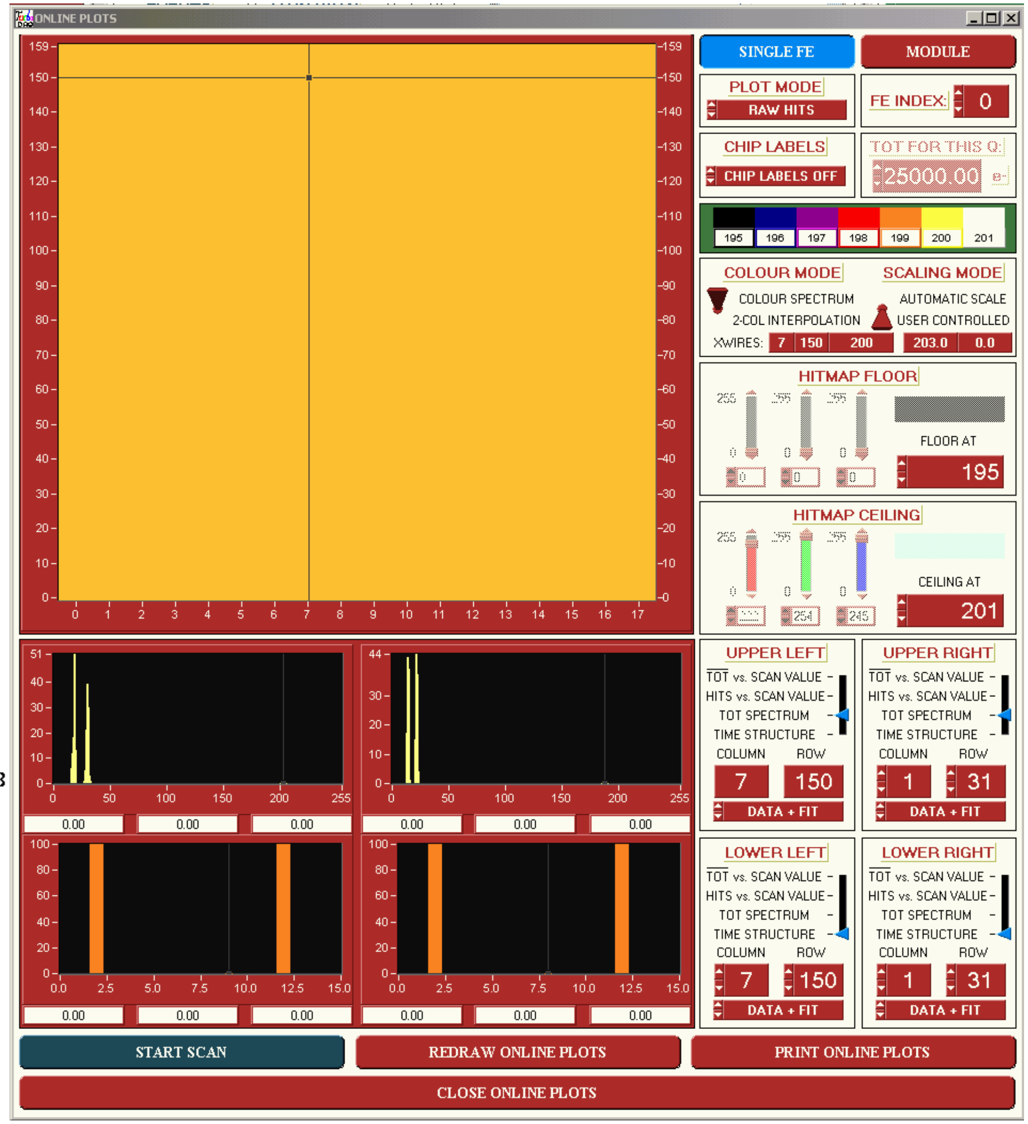




- In this case, the gap between pulses is 140ns, both the efficiency and the timing information are now always good.

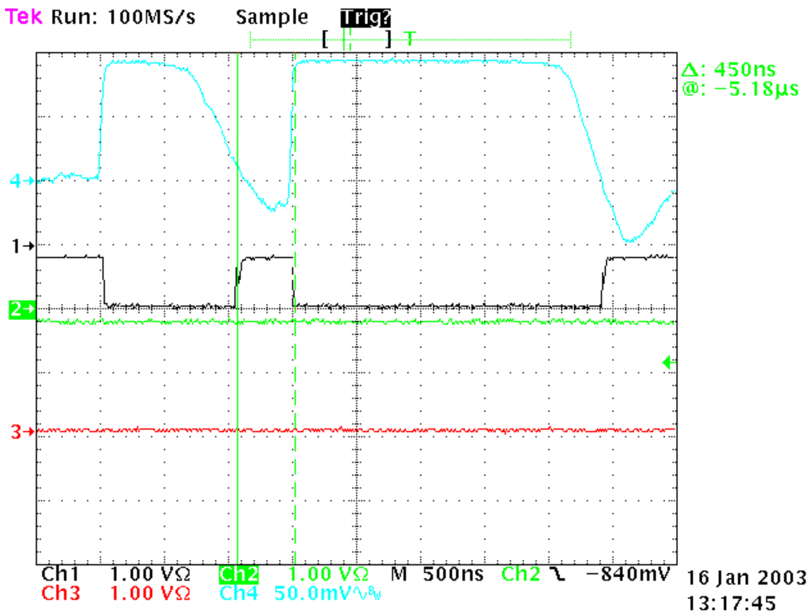
- Example of injection into full array (9*10 pixels to read out, 30Ke and 80Ke):

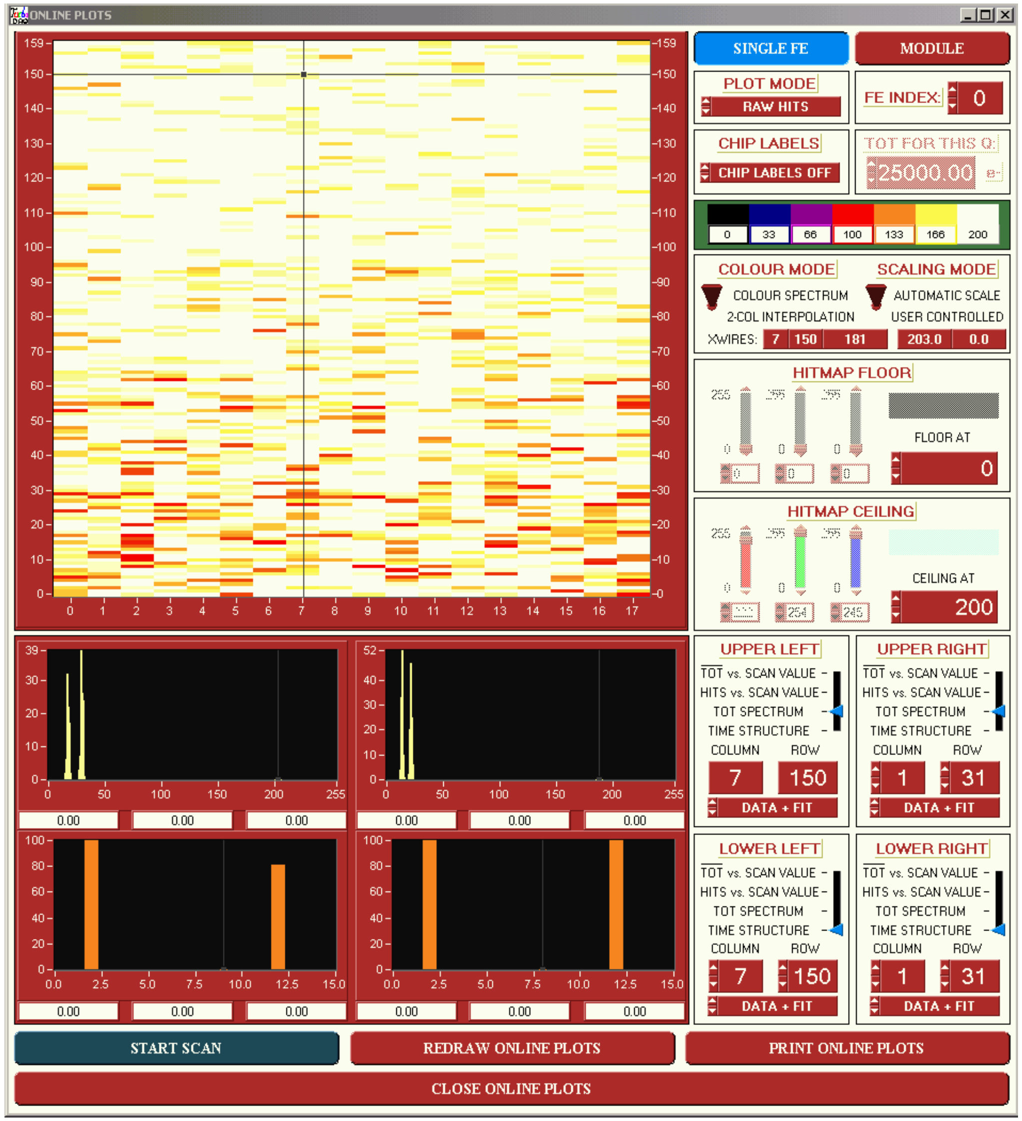




- In this case, the CEU=40MHz option was used for the readout, the gap between pulses is about 450ns. The efficiency and the timing information are always good for the full array.

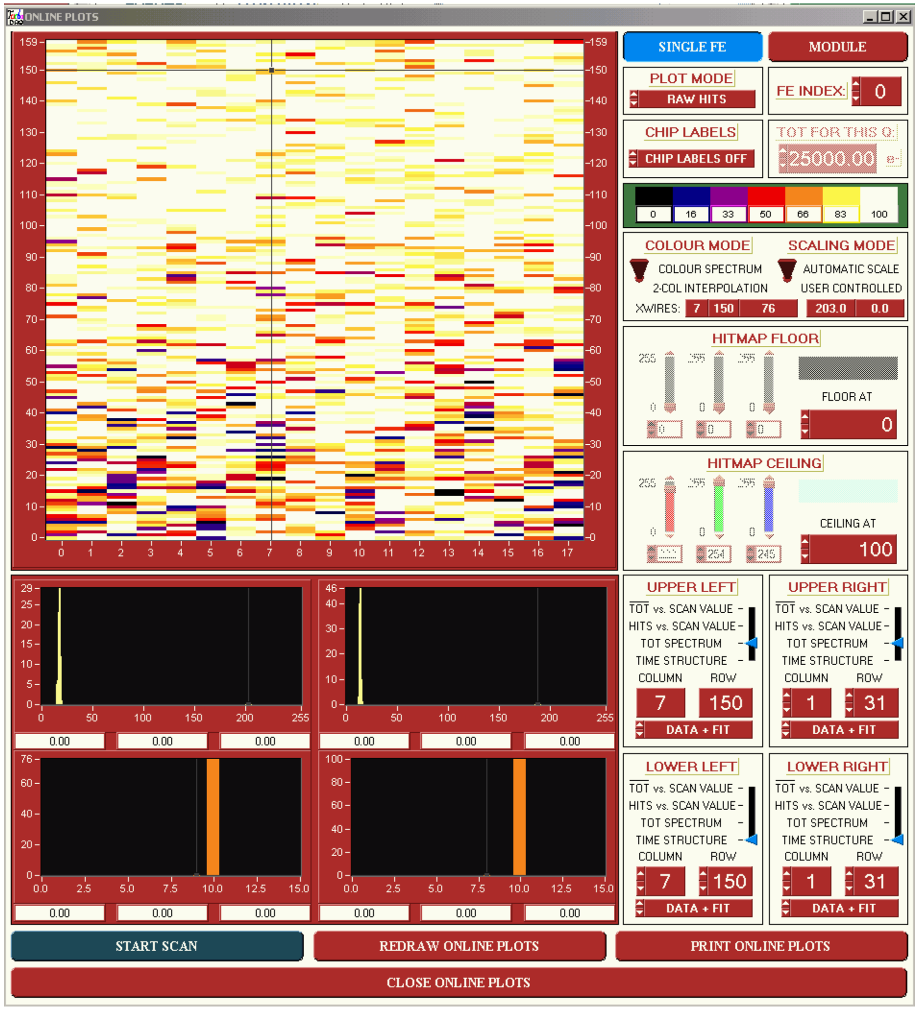
- Example of injection into full array (9*10 pixels to read out, 30Ke and 80Ke):

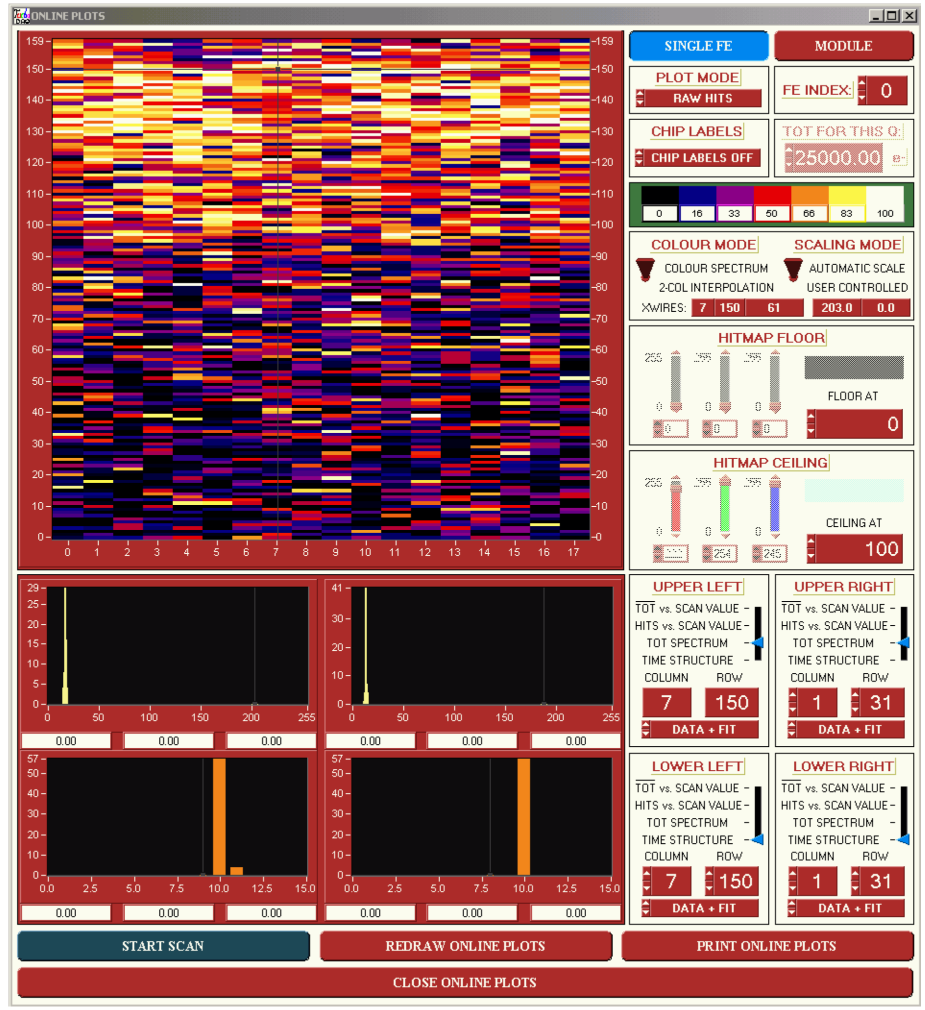




- In this case, the CEU=20MHz option was used for the readout, the gap between pulses is about 450ns. The efficiency is reduced by the fact that there is not enough time to read out one hit before the second one arrives.

- Use TPLL Event Filter to look at performance of second pulse alone:



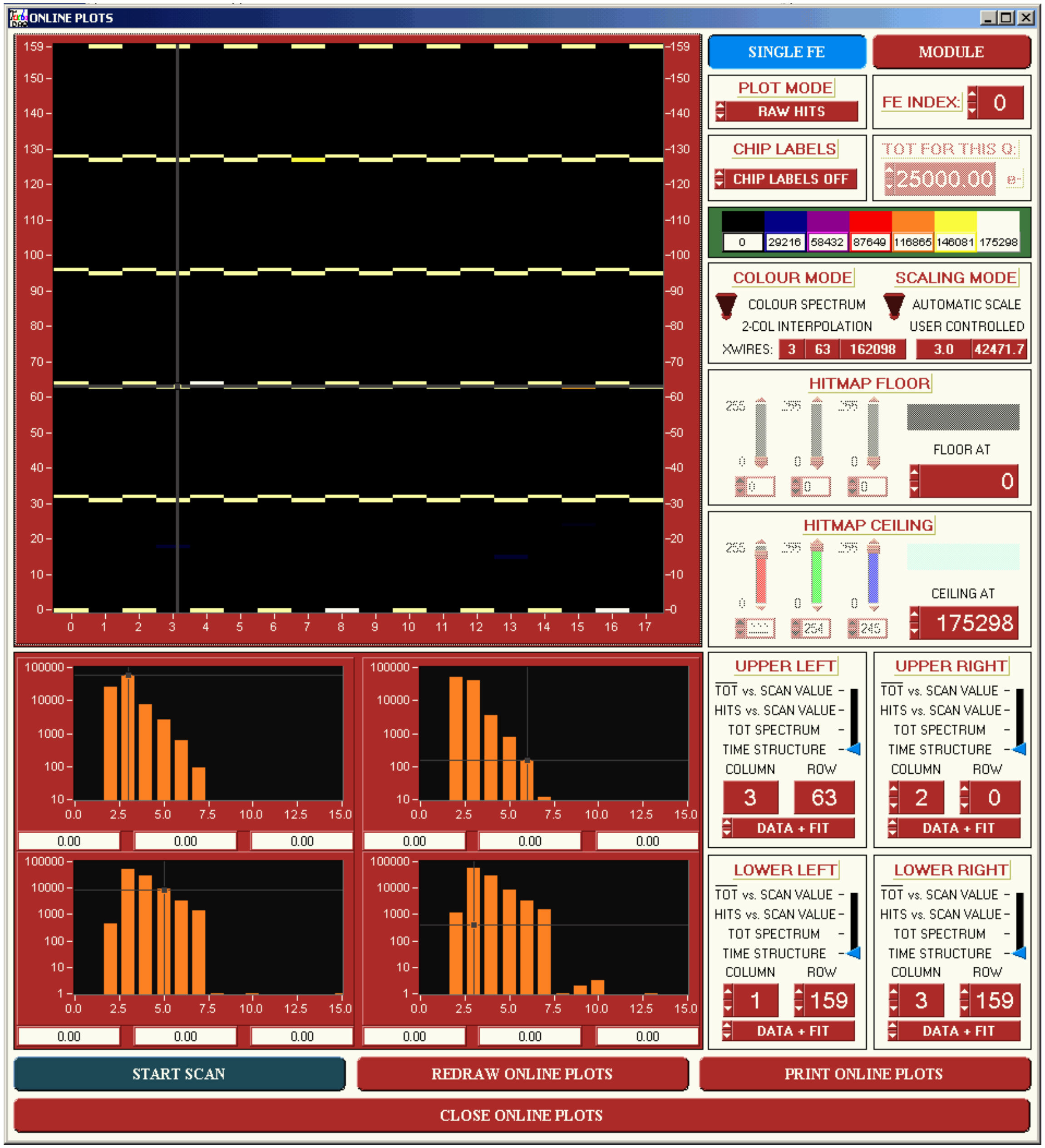


- Left TDAQ output is for CEU=20MHz, right TDAQ output is for CEU=10MHz. The data for the first pulse is perfect.
- Conclude that readout of double hits performs as expected. The use of CEU=40 helps considerably in clearing the hits from the pixels as rapidly as possible.

Double Trigger Group Studies

- Perform studies with two groups of triggers, separated by a programmable gap. This uses features implemented in TPLL V13 and TDAQ3.4.
- First use this to look for extra noise or digital cross-talk in a single chip assembly associated with the intense digital activity of event readout. The second group of triggers is shifted to overlap different phases of chip readout for hits associated with the first group of triggers.
- Use a low-threshold tune of 2Ke to enhance the sensitivity. This particular tune had 6 pixels with a threshold below 1Ke, and only these pixels showed interesting results in the second group of triggers. This already indicates that the digital crosstalk in FE-I1 is very small.
- Perform a threshold scan with the charge injection timed to produce hits starting in the third trigger accept of the first group. The scan was done in “readout all” mode (stage only the Select mask, set Readout mask to all 1). The second group of triggers was placed at 128 crossings after the initial trigger group (all readout finished within the pixel array) or at 50 crossings (TOT at end of scan is about 25, and 32_step scan with CEU=20 requires 40 crossings to readout, so this is in the middle of the column readout activity).

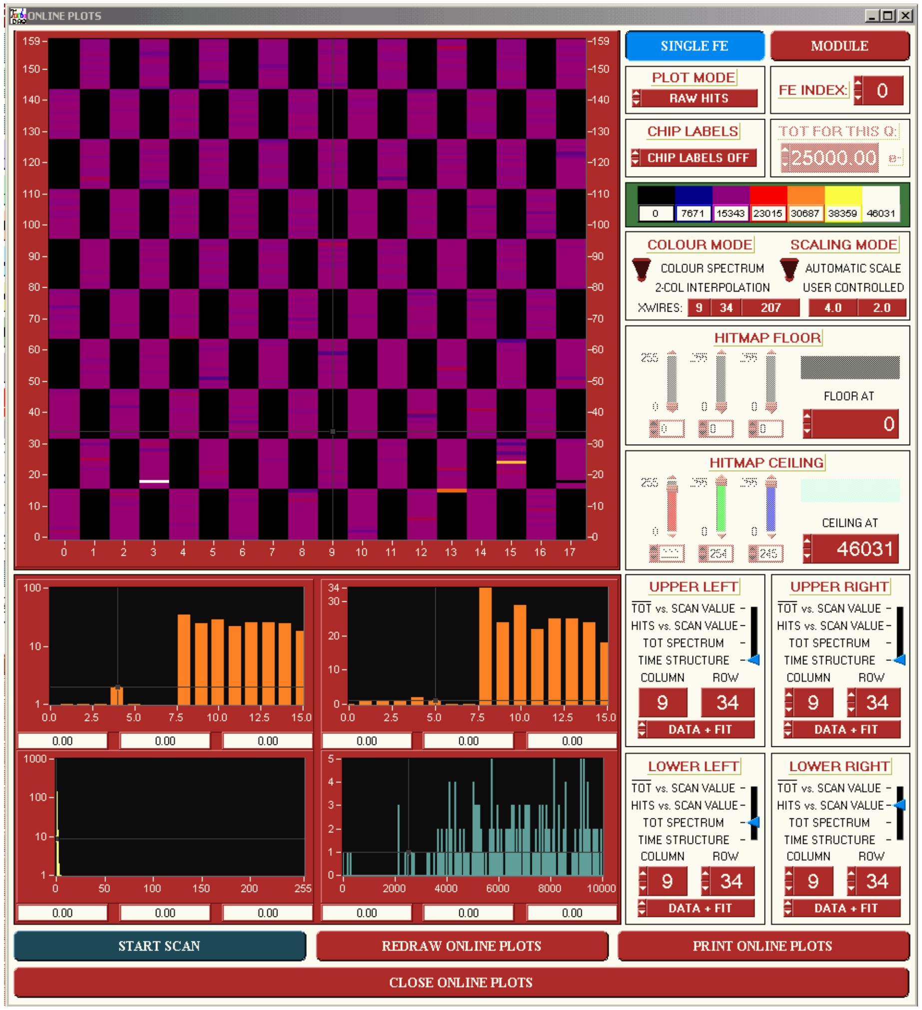
• Readout all scan of IZM_B with 2Ke threshold and 1K events per VCal value:

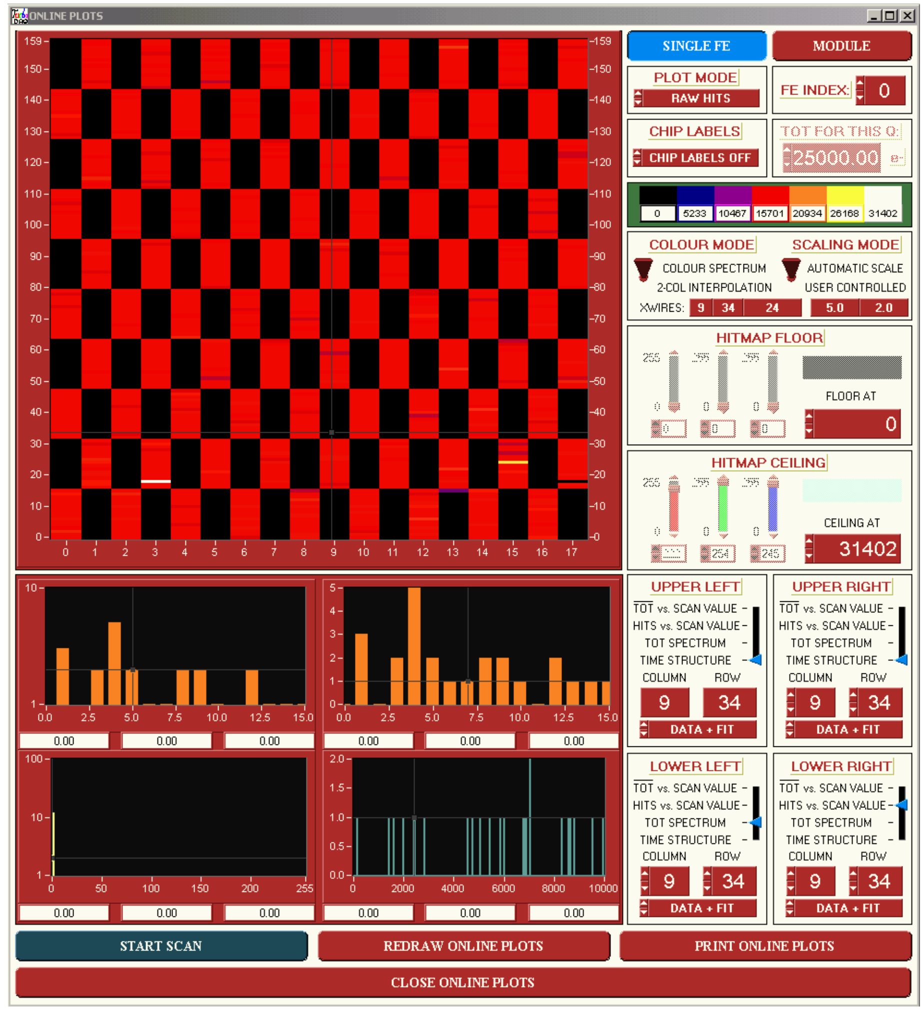


Scan results are very clean, even with low threshold in readout all mode.

Note that some hits appear even up to five crossings after the "high charge" hits, due to the large timewalk for hits right at threshold (note the log vertical scale !)

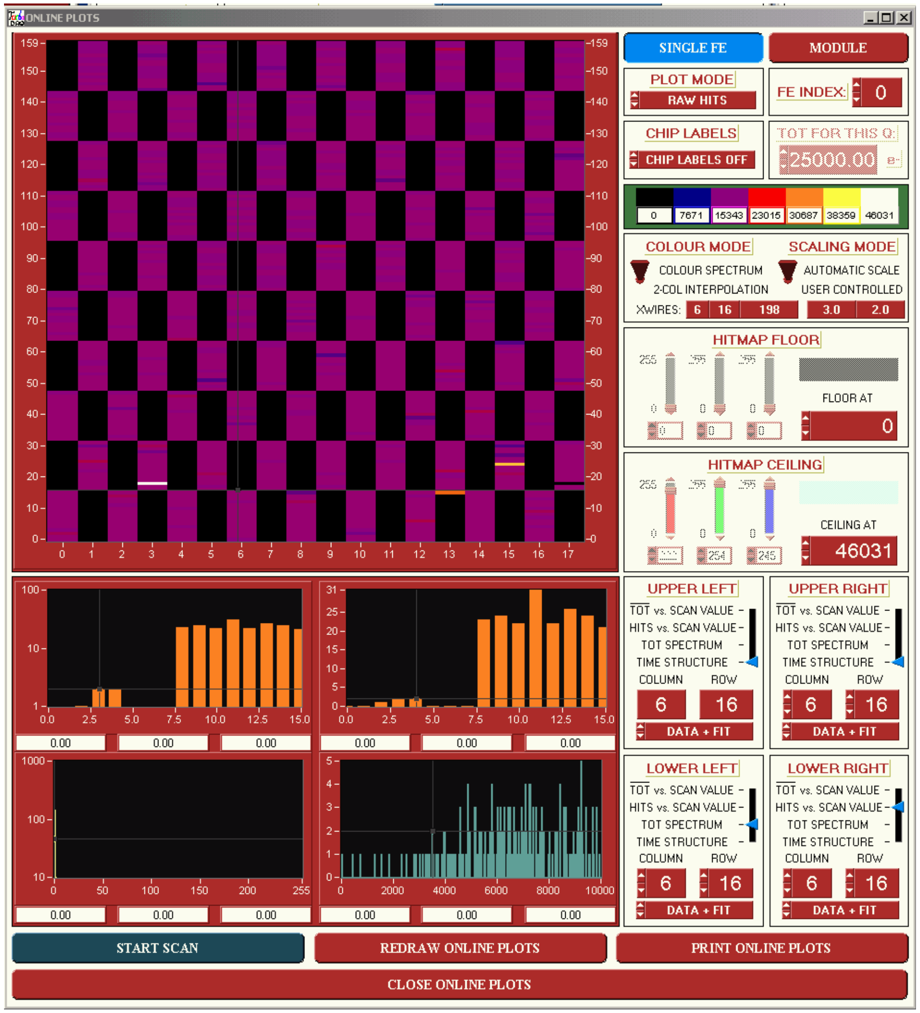
- Comparison of results for pixel (9,34) with gap of 50 (left) and 128 (right) crossings:

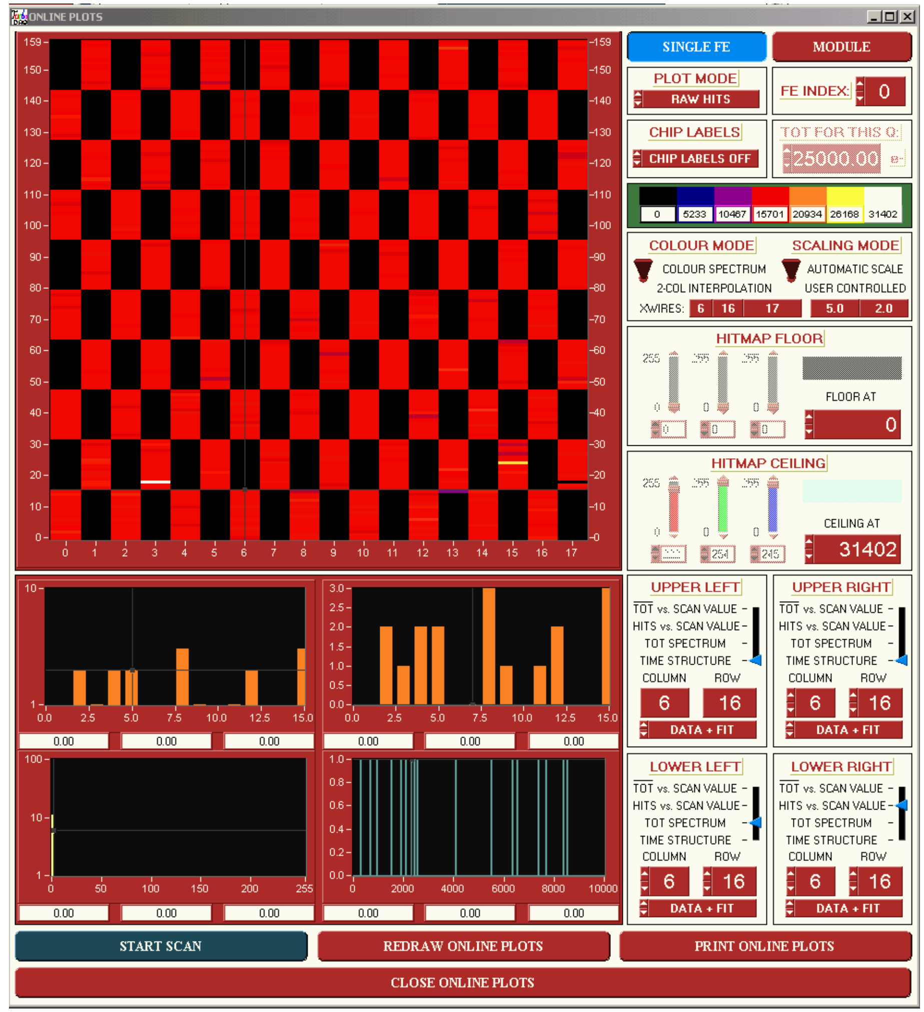




- This pixel has a threshold of 835e. It shows a low rate of uniformly distributed hits (first group of 8 triggers, and second group after 128 crossings).
- For the gap of 50 overlapping the column readout, there is a significantly higher hit rate (25 hits/crossing in a scan of 1000 triggers and 200 VCal steps).

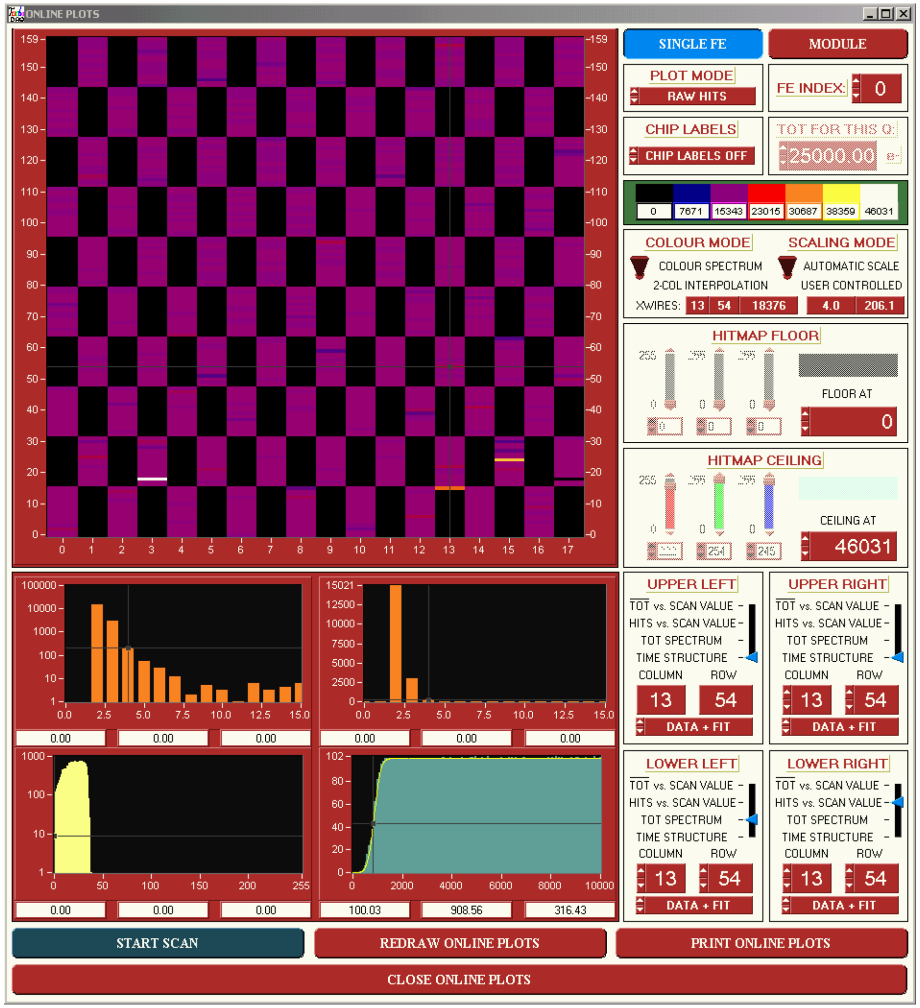
- Comparison of results for pixel (6,16) with gap of 50 (left) and 128 (right) crossings:

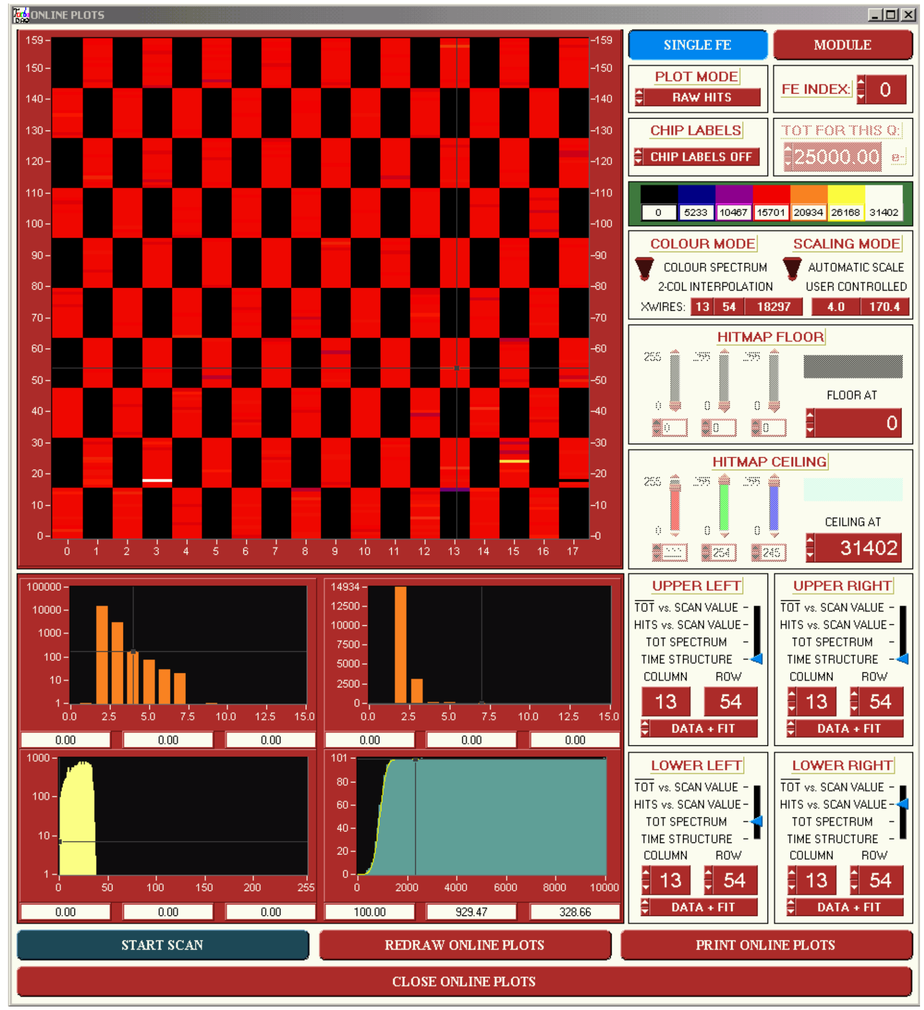




- This pixel has a threshold of 881e (only two pixels with threshold less than 800e). It shows the same behavior as pixel (9,34)
- For the gap of 50 overlapping the column readout, there is a significantly higher hit rate (25 hits/crossing in a scan of 1000 triggers and 200 VCal steps).

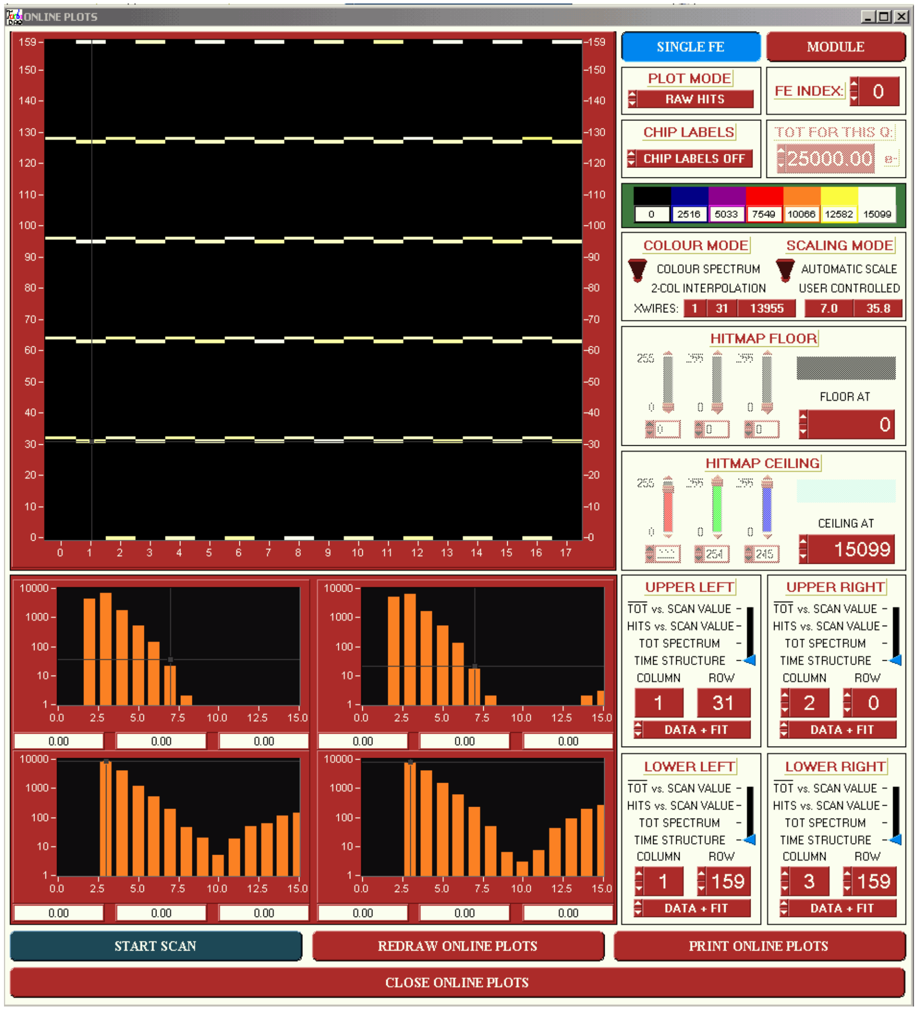
- Comparison of results for pixel (13,54) with gap of 50 (left) and 128 (right) crossings

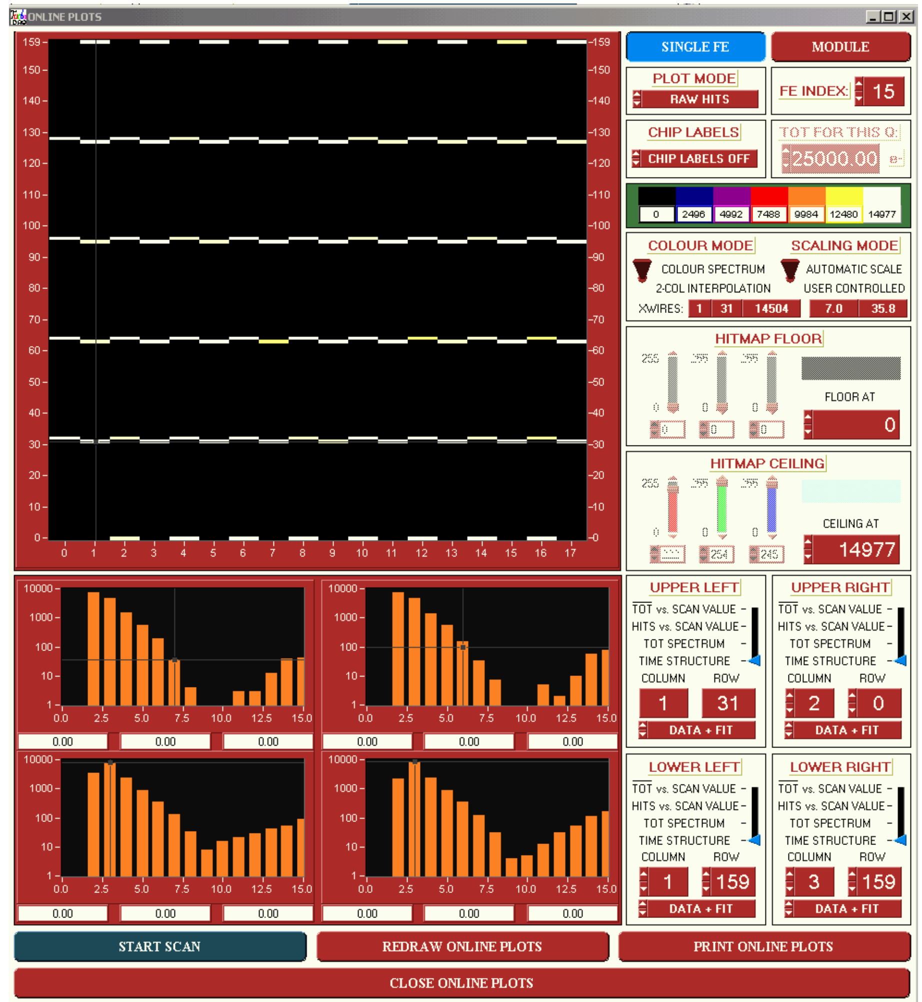




- This pixel has a threshold of 909e. It shows a low rate of uniformly distributed hits in the second group of triggers when they overlap the column readout period.
- None of the pixels with thresholds above 1000e showed any sign of activity associated with the second group of triggers.

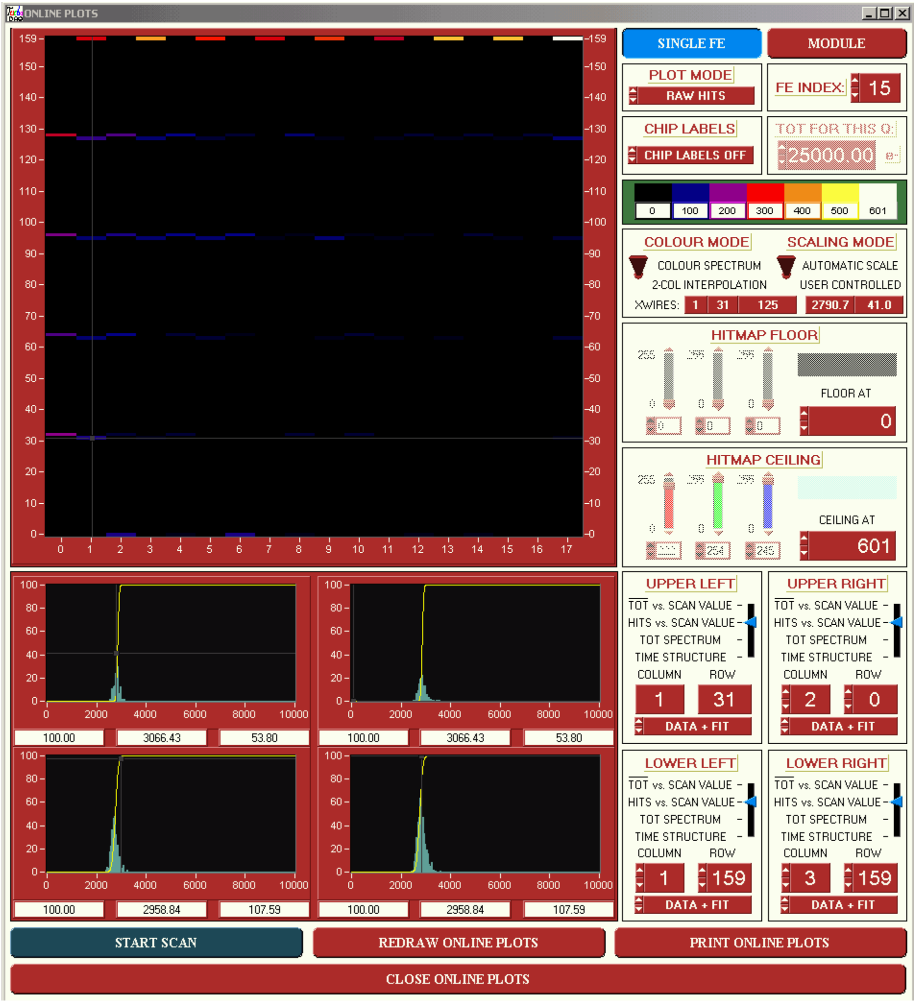
- Study LBL_4 module in concurrent mode with 3Ke threshold (NOT readout all):

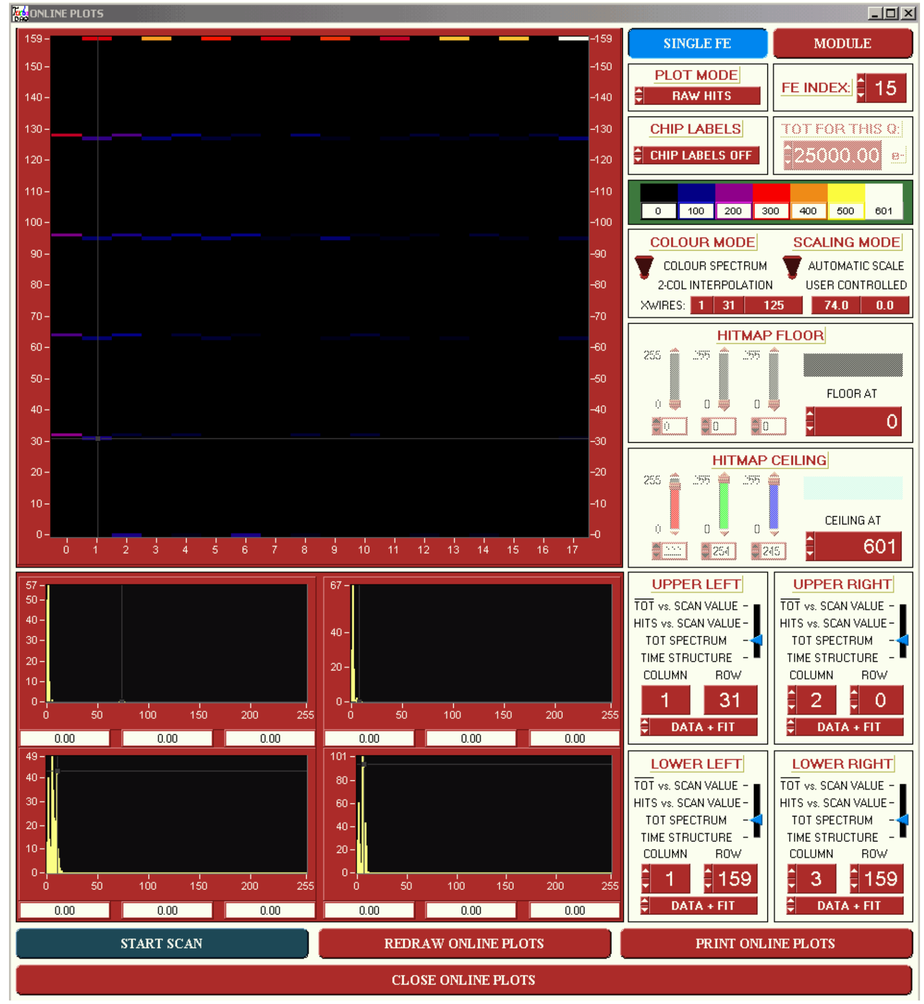




- Scan was done with a contiguous set of 16 accepts. Results for chip 0 (left) are “typical”, some chips show less activity, and chip 15 (right) is a “worst case”.
- See many extra hits after the nominal end of the initial hits. Ganged pixels show much greater activity.

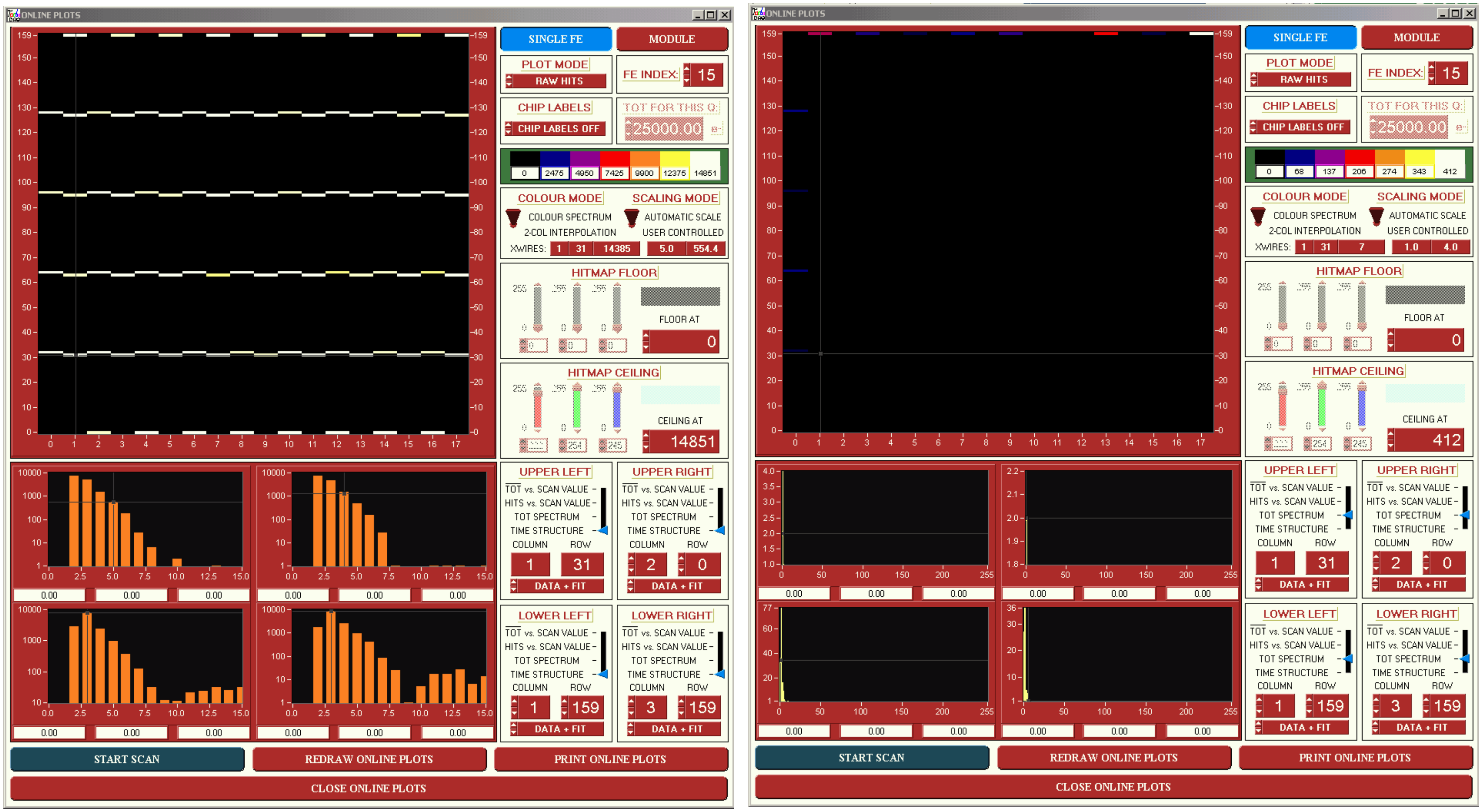
- More details for chip 15, using event filter to eliminate hits in first 10 crossings:





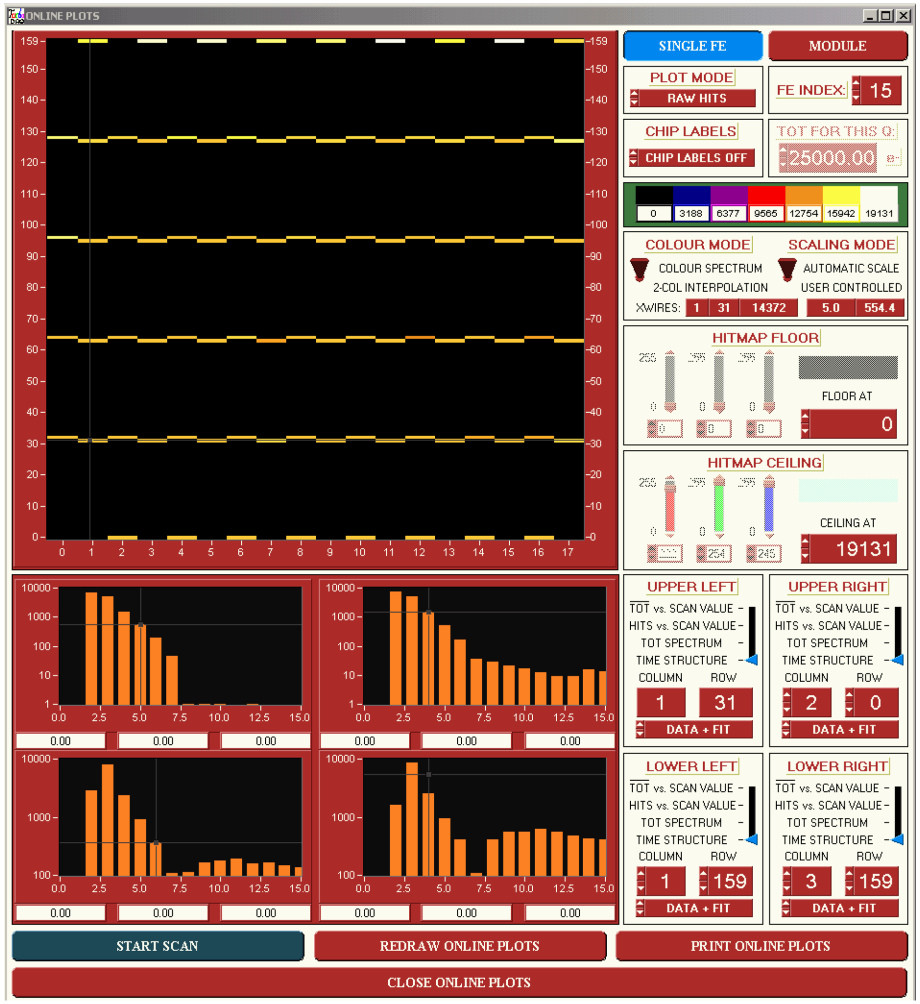
- This makes it clear that for 16 contiguous crossings, the extra hits are all associated with the part of the scan with the charge very close to threshold.
- For the normal pixels, the TOT of the second hit is very small (2-3), whereas it is larger for the ganged pixels due to their higher noise. This is "after-pulsing". Note that this small TOT can be eliminated using the TOT processor without side-effects

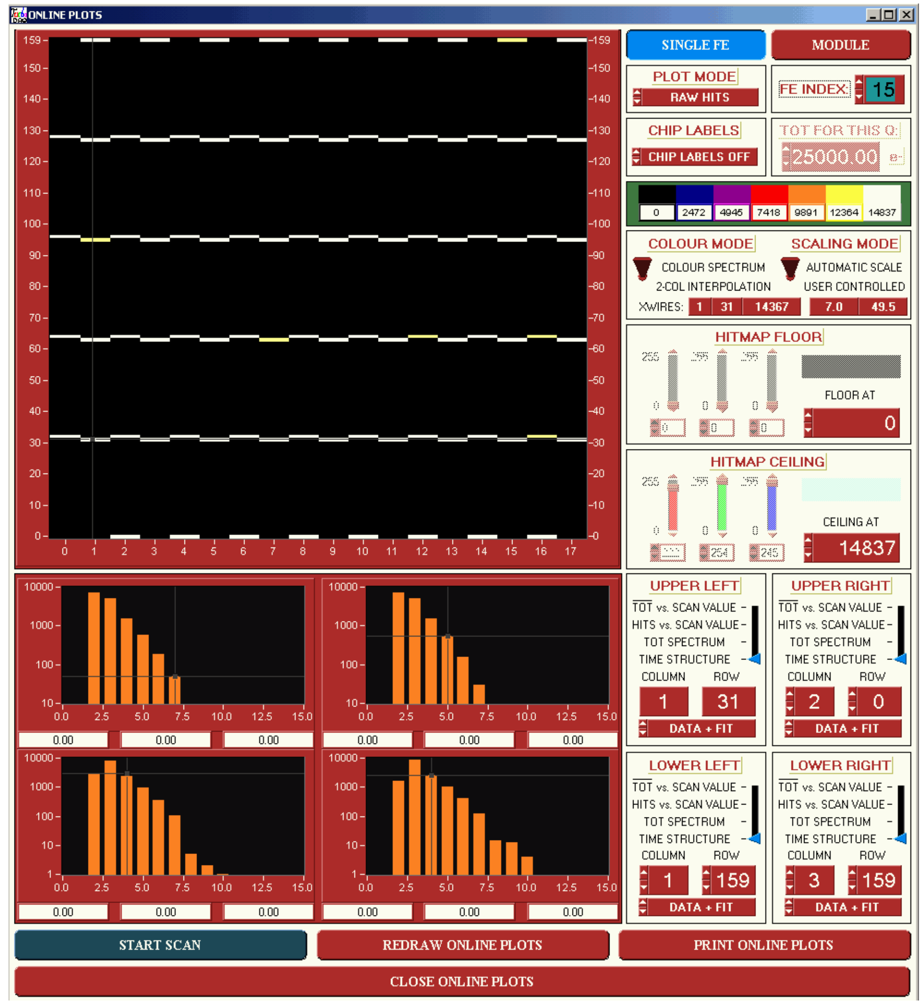
- Number of extra hits is significantly reduced in single FE mode:



- The TOT distribution for the extra hits is very strongly peaked towards very low values (few counts), even for the ganged pixels.
- The after-pulsing seems to be related to the amount of activity on the module (and it is not present at all on a single chip assembly). Concurrent mode is 1440 hits, which is a very unusual level of simultaneous activity.

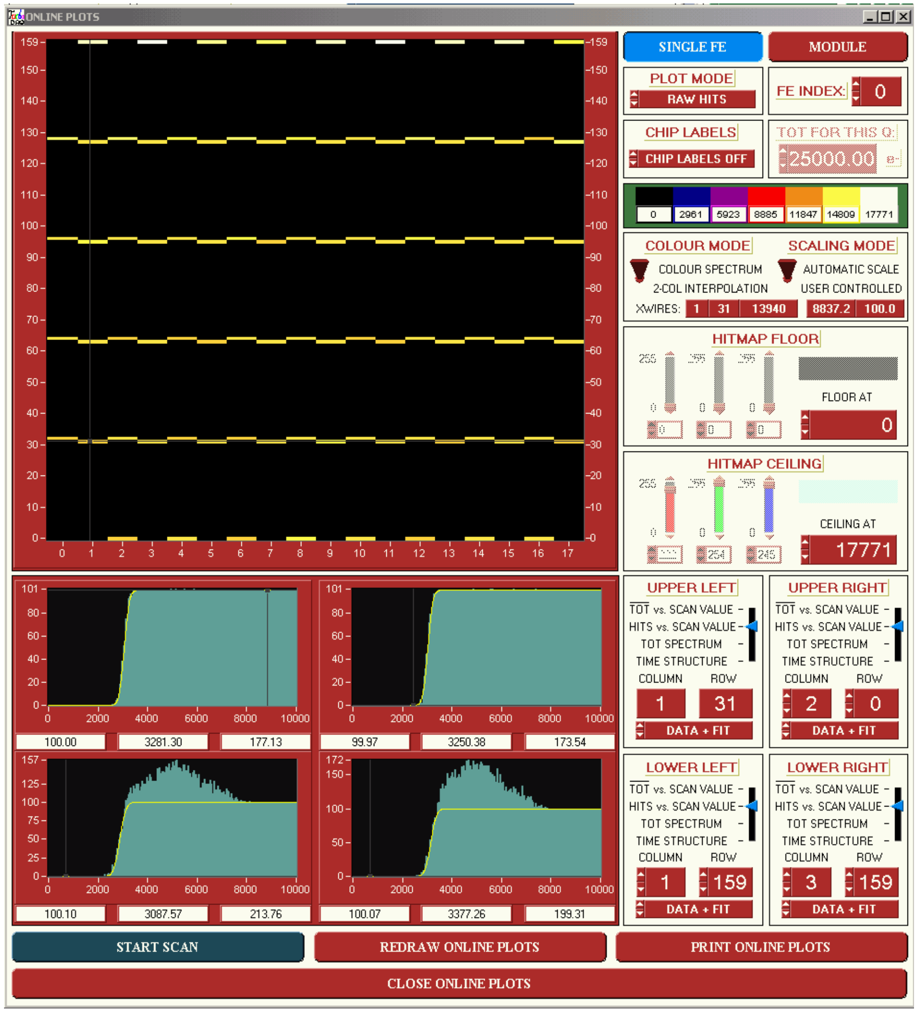
- Look at chip 15 with a gap of 20 and 40 crossings between trigger groups:

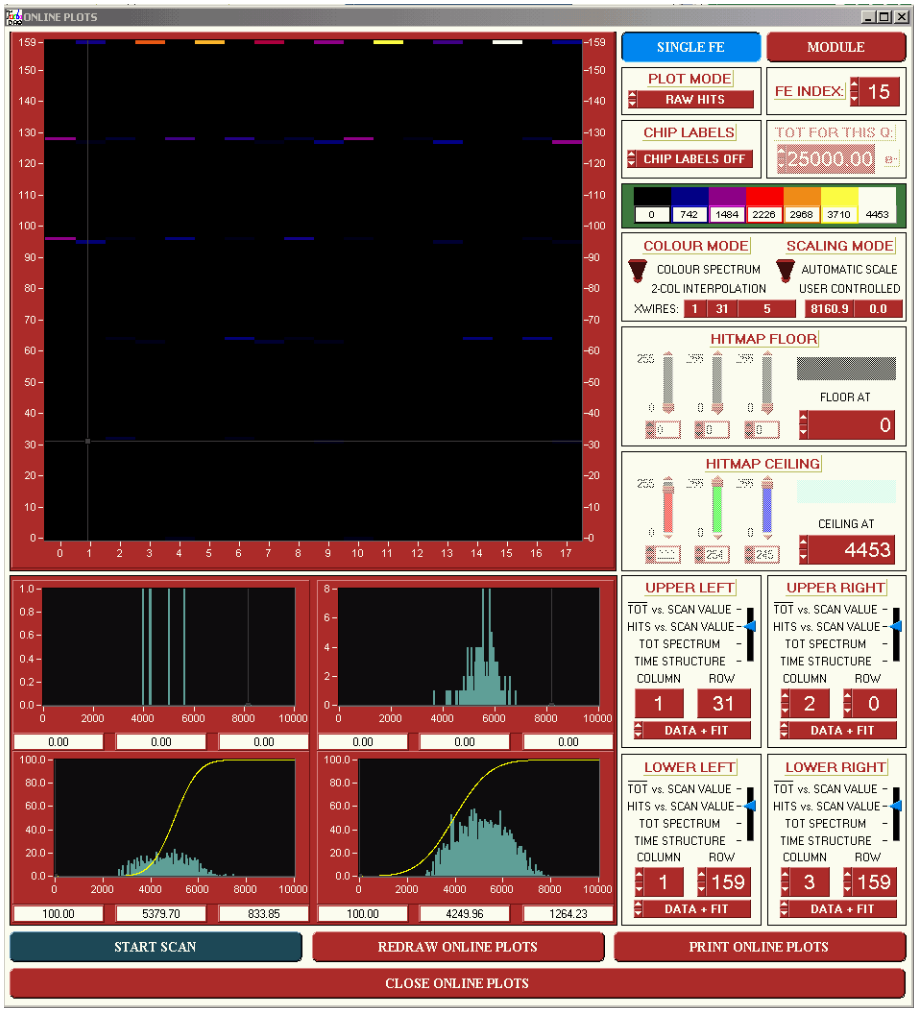




- See very significant activity for gap of 20, but almost none for the larger gap. Note the larger gap places the second group of triggers somewhat after the end of the largest TOT (roughly 30 for this scan).
- This is different from low-threshold single chip pixels (digital crosstalk during column readout), and corresponds to after-pulsing (not seen in single chips ?)

- More details for chip 15 with gap=20, with and without the event filter:





- The extra hits are now associated with a later part of the scan. Note that there are a large number of these hits in the ganged pixels.
- The TOT distribution for the extra hits is still peaked towards very low values (few counts), even for the ganged pixels.

Summary of double trigger group studies:

Single chip studies:

- For single chip studied, there is evidence for digital cross-talk caused by the activity of the column readout. However, it only occurs for the most extreme threshold conditions of roughly 800-900e thresholds, and even then only at a relatively low rate.

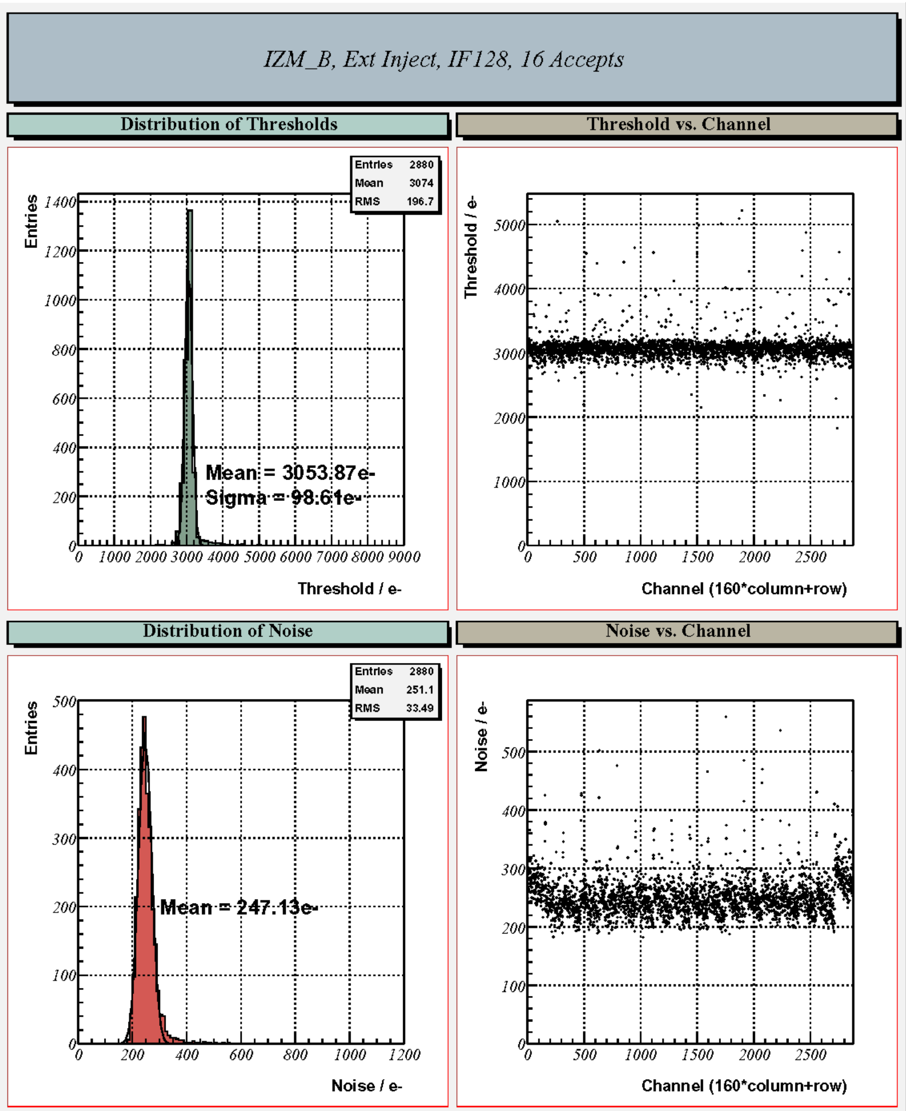
Module studies:

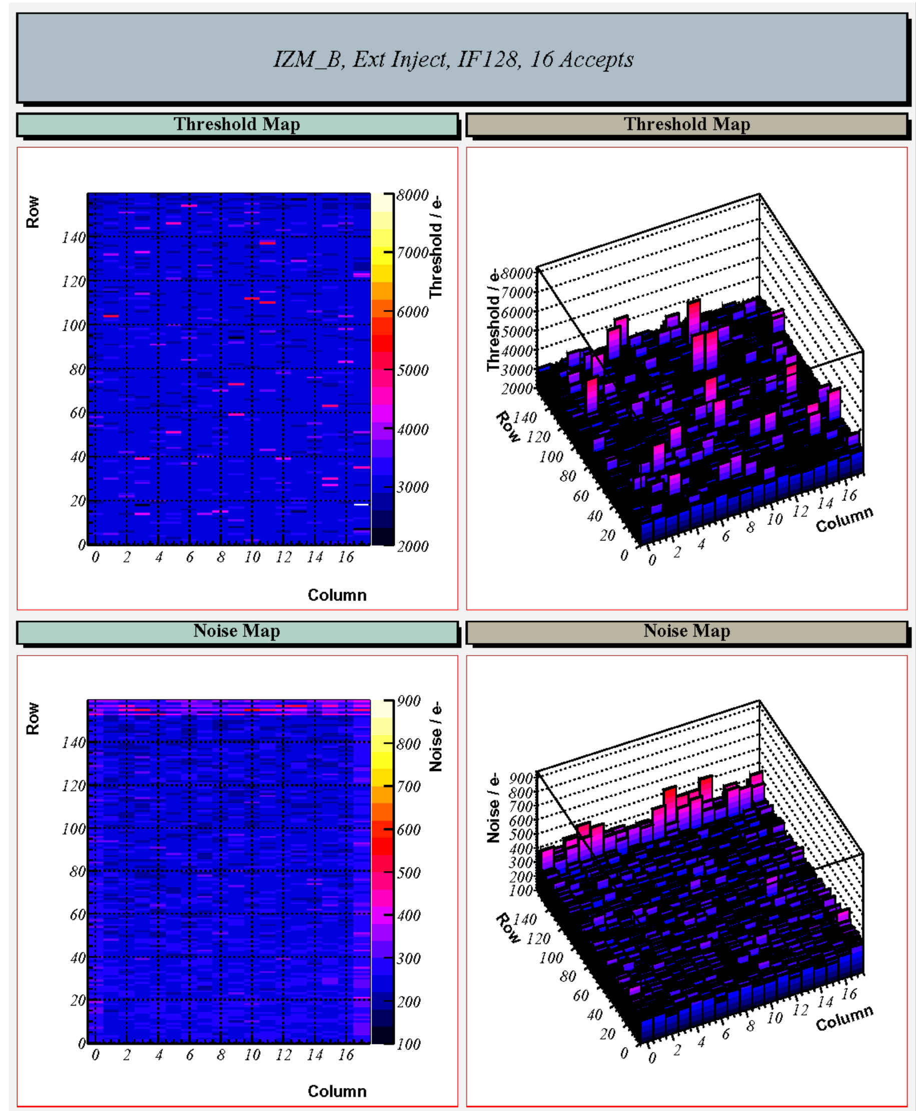
- For the module studied, there is evidence for after-pulsing. This means that, with a relatively low probability, a normal hit is followed by a second, small TOT pulse.
- This is expected at some level in our design, as there is no hysteresis in the discriminator, and the constant-current feedback produces a relatively slow return to baseline.
- The rate seems related to the amount of activity in the module. Single FE chip threshold scans (90 simultaneous hits injected) produce minimal after-pulsing. Concurrent threshold scans (1440 simultaneous hits injected) produce significant after-pulsing, especially in the ganged pixels.Many of these hits could be eliminated by the use of the TOT processor with a low threshold cut.
- Further studies needed to assess how large an operational problem this poses. However, it looks managable (no major problems seen in source scans, some evidence seen in H8 noise occupancy studies).

In-time Threshold Studies

- Use event filter to study single crossing threshold performance (FE-I1 readout for single crossings is not reliable due to ROC bug).
- First, perform standard “16 accept” threshold scan, where the highest charges typically appear about the middle of the 16 accepts.
- Then, use a 100Ke charge and scan the strobe delay to establish when the hits from this large injection are just barely associated with a given crossing. This is the type of procedure which will be used to adjust the timing in ATLAS.
- Use the same strobe delay (about 180 counts or 118ns in this case) to perform a threshold scan. This corresponds to allowing 25ns for timewalk from 100Ke down to the in-time threshold.
- Also perform scans with strobe delays of 170 counts (corresponds to about 32ns of allowed timewalk relative to 100Ke) and 190 counts (corresponds to about 18ns timewalk relative to 100Ke).
- Present studies were done with a single chip for simplicity. Will be extended to full module studies as well.

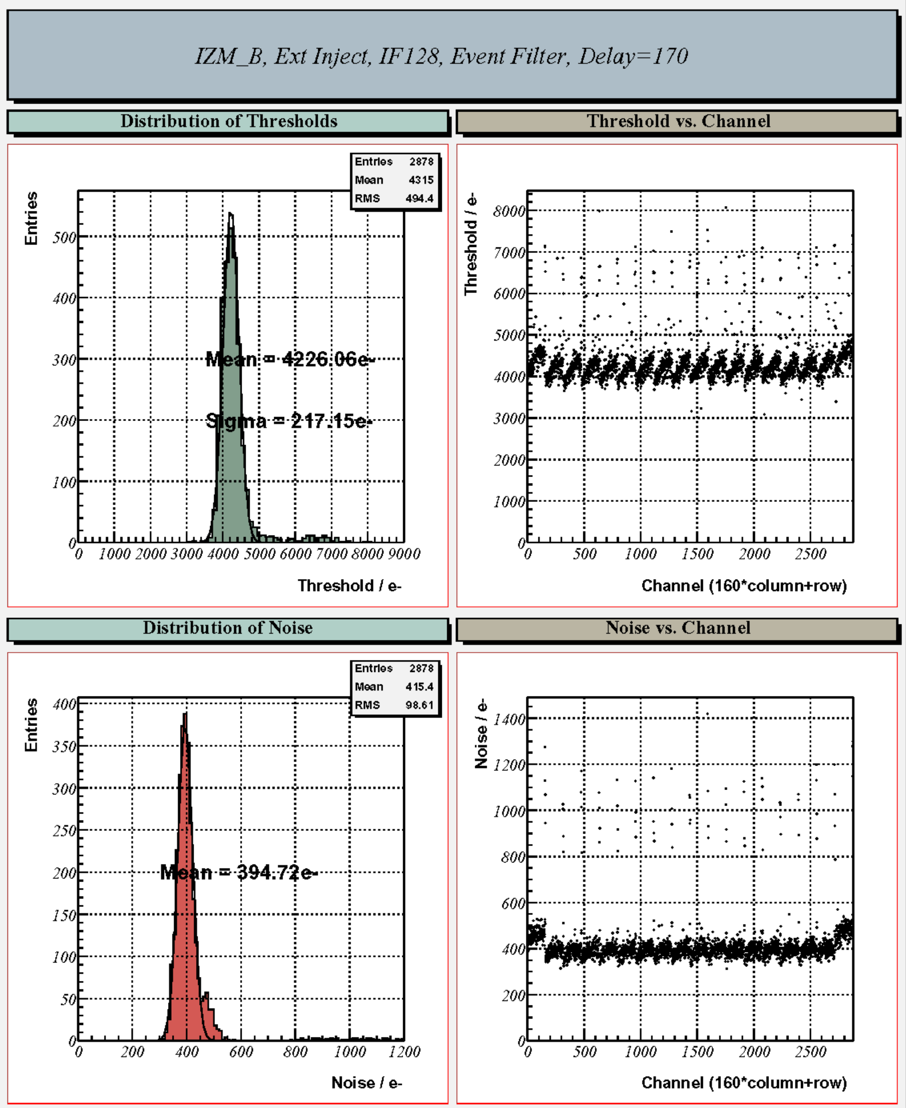
- Initial threshold scan (16 accepts):

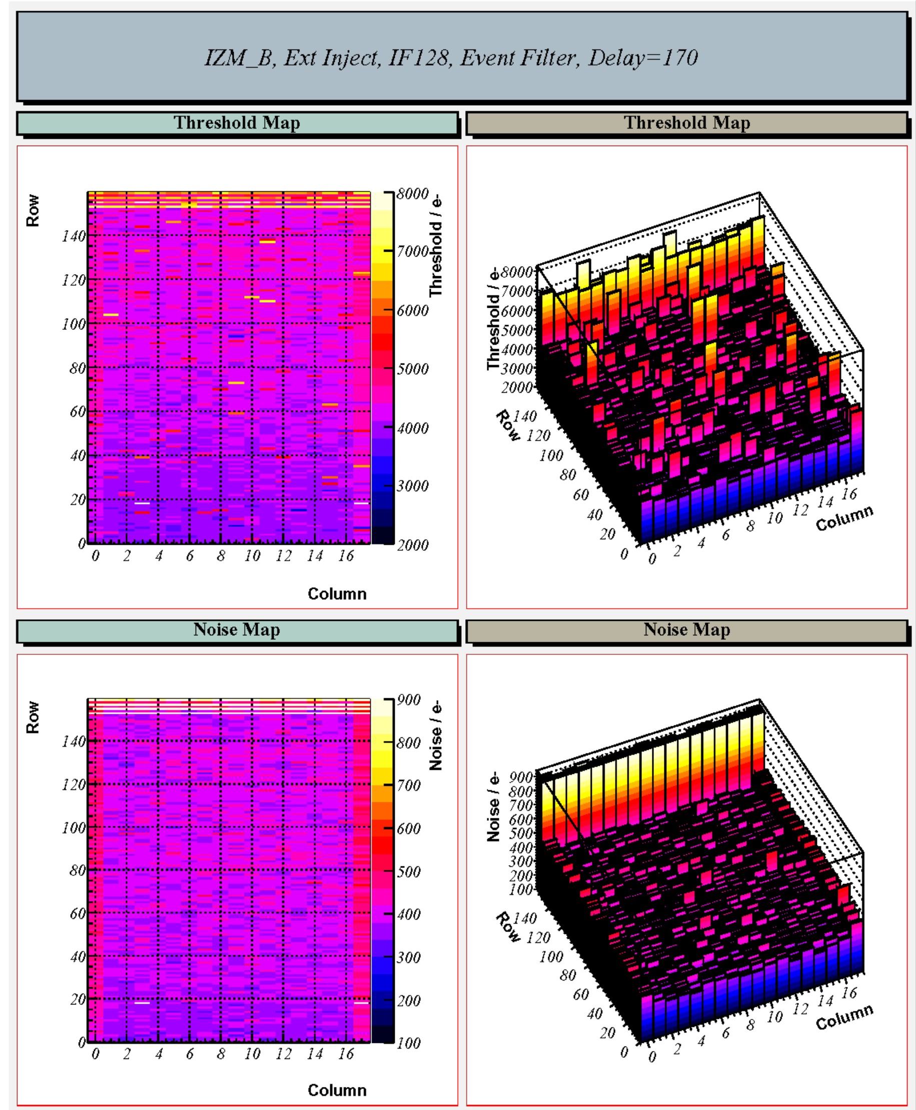




- Typical uniform threshold with 90e dispersion and 250e noise (before TDAQ bug fix).

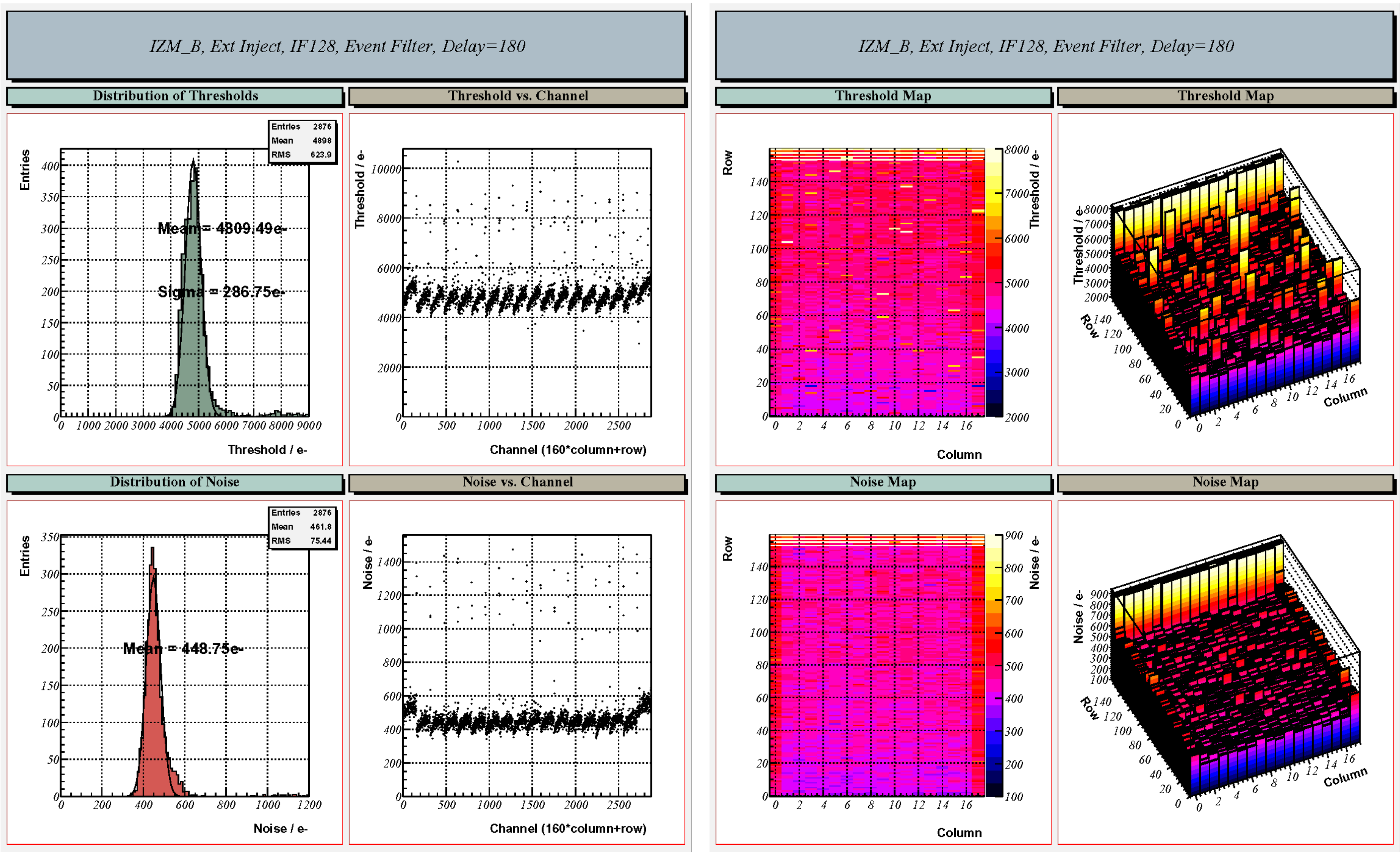
- Single crossing threshold scan using event filter and delay=170 (32ns timewalk):





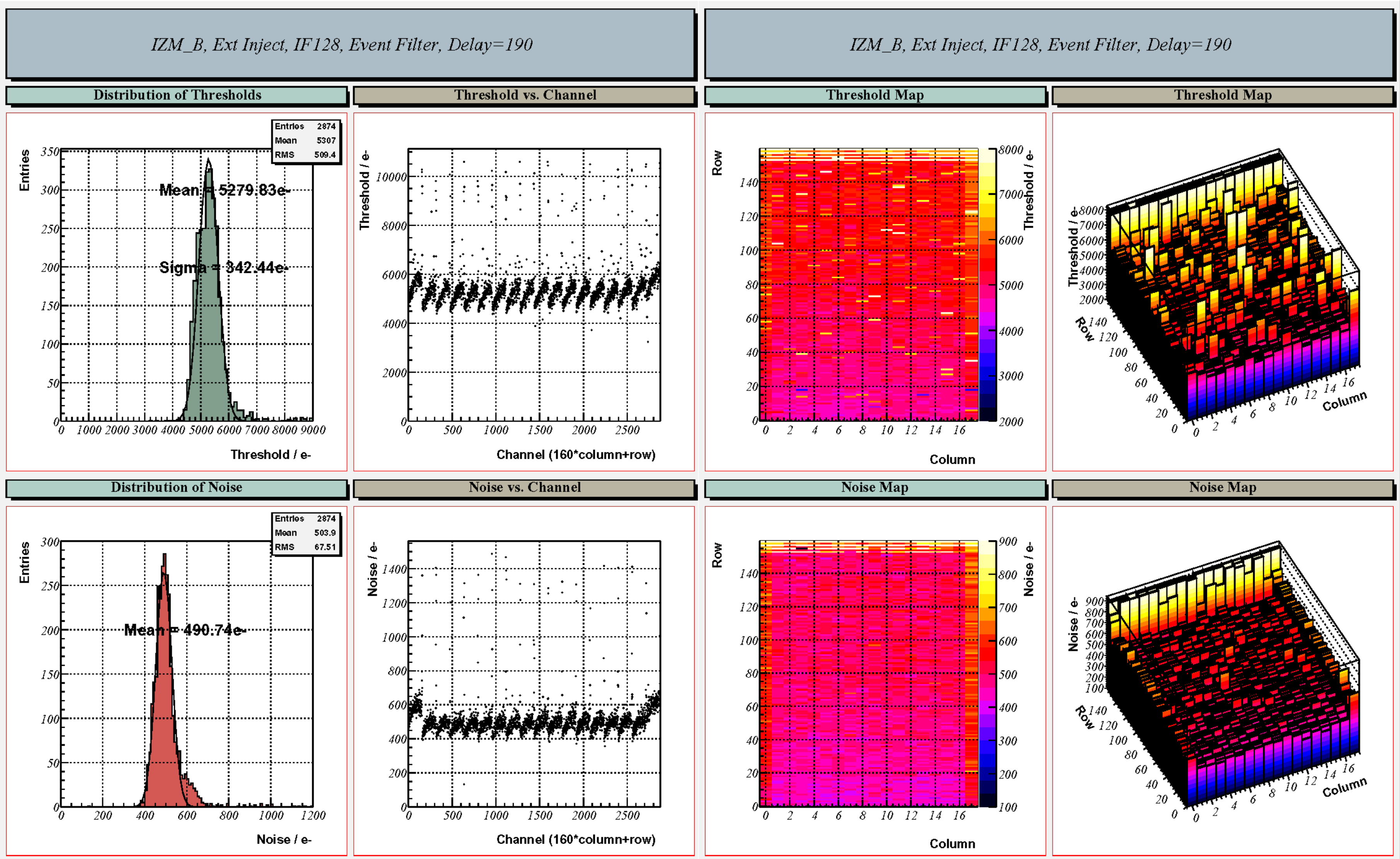
- The threshold has increased by 1200e. There is significant threshold variation along the column, due to non-uniform IP distribution which in turn degrades the timewalk. The apparent noise has increased due to convolution with timewalk.

- Single crossing threshold scan using event filter and delay=180 (25ns timewalk):



- The threshold has increased by 1750e. The threshold variation and apparent noise have both increased somewhat further compared to the previous scan.

- Single crossing threshold scan using event filter and delay=190 (18ns timewalk):



- The threshold has increased by 2200e. The threshold variation and apparent noise have both increased somewhat further compared to the previous scans. The measured overdrive from a timewalk scan (20ns timewalk) is similar to this value.

Problems with Module Readout

- During the previous measurements looking at performance of modules in "readout all" mode, there were problems (no results shown).
- The measurements are complex, and some of the problems may be related to software. However, there seems to be a problem with the MCC as well.

Module "readout all" mode:

- In this mode, all pixels in the module are enabled for readout, whether they are injected or not. The FE chips have buffering for up to 576 hits, while the MCC has buffering for only up to 112 hits per FE. Therefore, we should expect to see buffer overflows in the MCC if there are many extra noise hits.
- However, the MCC has been designed to handle this, and so it should not cause problems as long as we never send more than 16 triggers to the MCC at a given time. The MCC will simply ignore the extra hits until it sees an EOE word.
- This can be assured by waiting for a long enough interval between groups of triggers. The maximum interval should be given by the time to transfer 576 hits at 40Mbit/s (roughly 400μs) plus the interval to transfer 112 hits/FE at 160Mbit/s (about 300μs).
- For these studies, an interval of 3000 for the TPLL (corresponding to 1200μs) has been used, and the serial stream has been checked on a DPO scope.
- Nevertheless, see large numbers of "LVL1 match" errors from MCC.

Simplified tests:

- The previous threshold scan tests were done in part because they provide large amounts of data scattered across several trigger accepts in a somewhat random way, and therefore stress the module readout.
- A simplified version of these tests has been performed by using digital injection with a 20_step mask. This attempts to send 144 hits per FE chip instead of the 90 hits per FE chip sent with a 32_step mask. The tests were always in concurrent mode, so all chips are sending excess data.
- Already in this case, one sees the same problem. Strangely, one does not see a buffer overflow for each event (but only somewhere close to half this number), and one sees many LVL1 match errors.
- This is puzzling, since the MCC should be able to deal with this type of buffer overflow error without synchronization problems.
- Is it possible that the MCC LVL1 matching algorithm cannot keep up with the data volume in this case, and therefore produces spurious errors ?
- Also the data as seen by TDAQ seems to have problems with beam crossing association (hits are scattered among different trigger accepts), but this could possibly be a loss of synchronization between TDAQ and the MCC.
- Should try tests again with 40Mbit MCC output, and compare single FE and concurrent modes.
- Need to discuss this problem in more detail with MCC experts this week...

Whats Left in Characterization of FE-I1 ?

- Most measurements carried out, at least in preliminary form.
- Continue studies of timing margins of single chips and modules using PICT system. Concerned about relatively poor timing/power supply margins observed in present modules (presented in Dec). Given understanding of FE chip and MCC chip operating margins, this should not be the case.